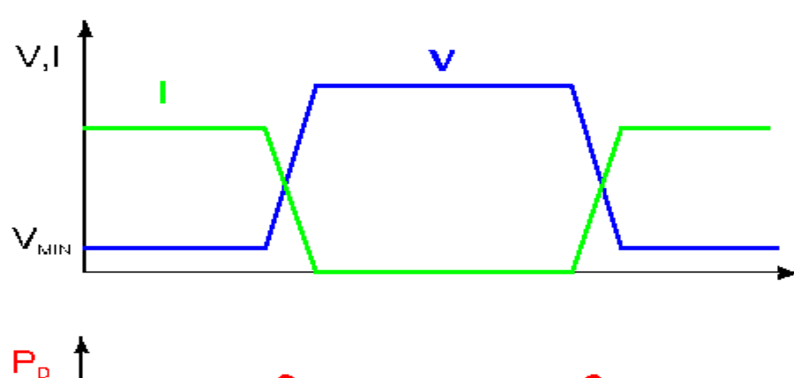
Power device ratings

What is the role of semiconductor devices in the power circuit operation?
As seen before, the performance of the power circuits is largely determined by the ratings of the power devices needed for the circuit operation, so it is of paramount importance to know the limits posed by the different power devices available, and to choose the right device for the required field of application.

The power efficiency η of the circuit is mainly determined by the amount of power dissipated in the power devices, (assuming the filter lossless): indicating as P_D the power dissipation in the device, we have:

$$\eta = \frac{P_O}{P_i} = 1 - \frac{P_D}{P_i}$$

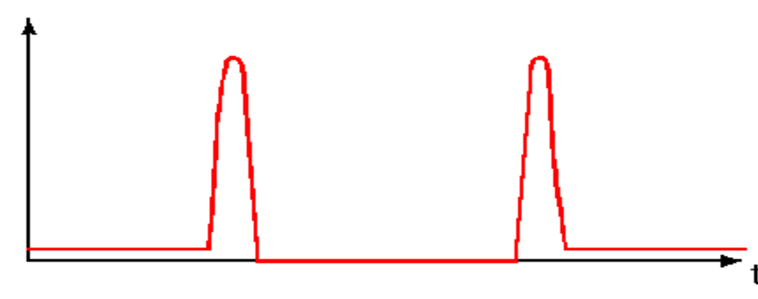


The power dissipation P_D, as discussed before, is the sum of the two components, the steady-state P_{DS}, and the dynamic P_{Dd} :

$$P_{DS} = \frac{1}{T}\int_{T_{ON}} p_{DS} = \frac{T_{ON}}{T} I_{MAX} \cdot V_{MIN}$$

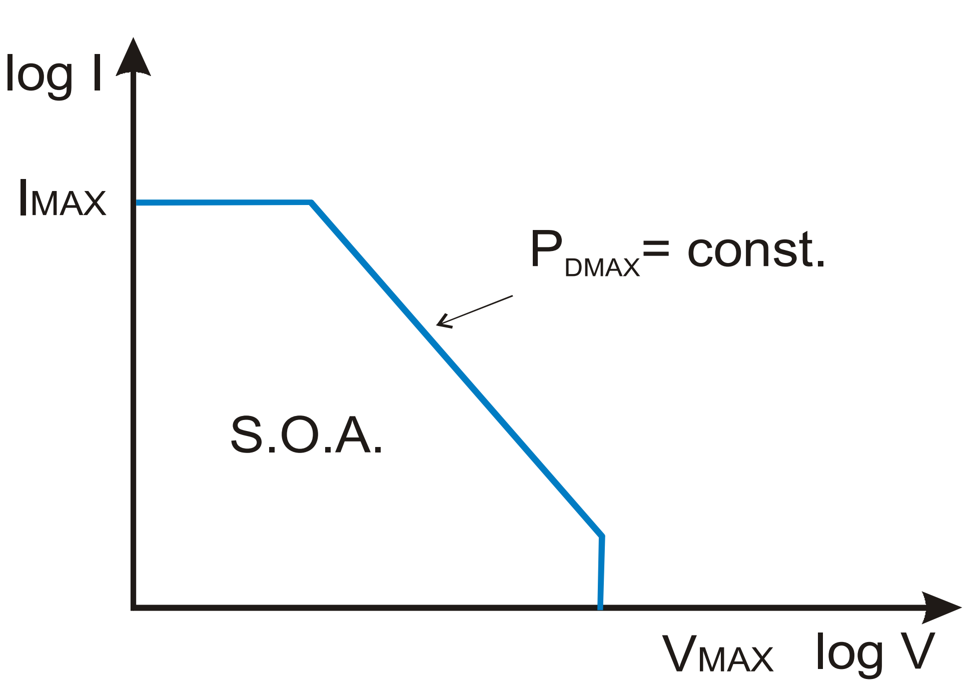
$$P_{Dd} = \frac{1}{T}\int_{\Delta T} p_{Dd} = \frac{1}{T}\int_{\Delta T} i(t)v(t)dt$$

P_{DS} and P_{Dd} are the average values over a single cycle, while p_{DS} and p_{Dd} are the values of instantaneous power)



Let's refer for the moment, to the steady state power dissipation P_{DS}. For most cases, the max power transferred to the output is dependent on the max values of power dissipation allowable by the device itself. All the devices show limitations both in max current, max voltage and max power dissipation.

These max ratings are usually conveyed in a surface in the output current/voltage coordinates (log) plane, defined as the Safe Operating Area (S.O.A):



We will discuss in detail the limitations posed on I_{MAX} and V_{MAX} by the different power devices, but let now concentrate on the P_{DMAX} limitations:

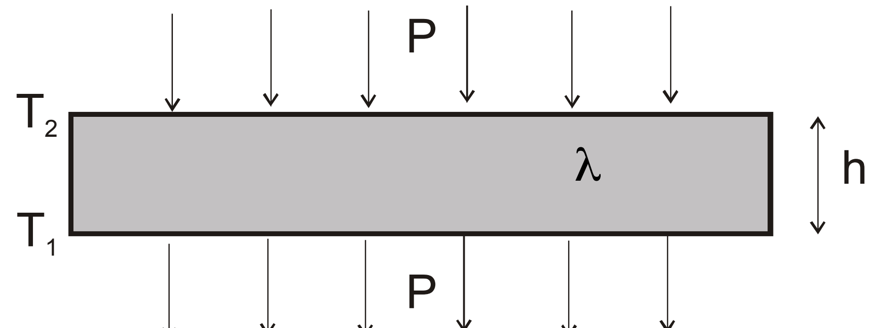
For most cases this value is dependent on the way the electrical power generated into the device is converted in thermal power by heating of the device. Then we must understand what is the amount of the power - P_{DMAX} - that can be dissipated without breaking the device itself.

D.C. power dissipation

The d.c. max power dissipation is dependent on the max temperature reached by the device in its operation. Then we must refer to some physics to define this temperature limit. Let's recall some basic equations of heat transfer in solids.

The heat Q is an energy (Mechanical equivalent in Joule)

The heat flow in the unit time through a surface S is indicated as P ; it is a thermal power (expressed in Watt)



In a metal plate of thermal conductivity λ the steady state heat transfer through the plate (in onedimensional analysis) is linked to the temperatures T_1 and T_2 of the two surfaces as:

$$P = \frac{\lambda S}{h}(T_2 - T_1)$$

$$\left[\text{in differential terms:} \quad dP = -\lambda dS \frac{dT}{dx} \right]$$

Thermal resistance

One can define the ratio $h/\lambda S$ as the thermal resistance R_T .

R_T gives the amount of the temperature difference between the two surfaces of the plate when a thermal power P is flowing through it, and it defines the capability of the plate, of area S, to allow the heat flow in it, if a surface (T_2) is heated with respect to the other one (T_1).

$$R_T = \frac{T_2 - T_1}{P} \qquad (1)$$

If the heat flow pass through more plates (with different h and λ) superposed each other, assuming again one-dimensional analysis, we have:

$$T_2 - T_1 = R_{T1}P; \qquad T_1 - T_0 = R_{T2}P;$$

$$T_2 - T_0 = (R_{T1} + R_{T2})P = R_{Ttot}P$$

$$R_{Ttot} = R_{T1} + R_{T2} = \sum R_{Ti}$$

P

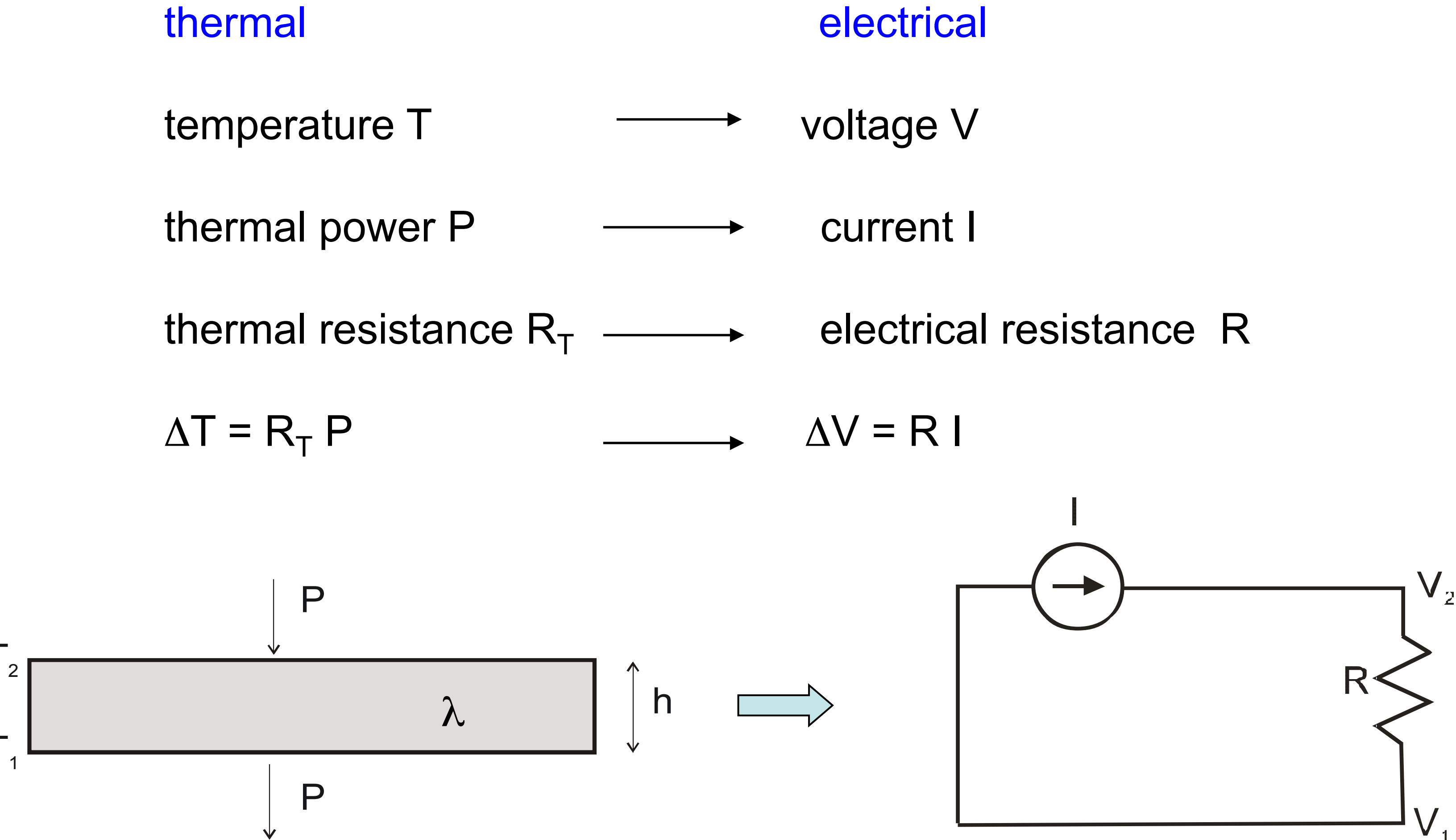
T_2 λ_1 h1

T_1 λ_2 h2

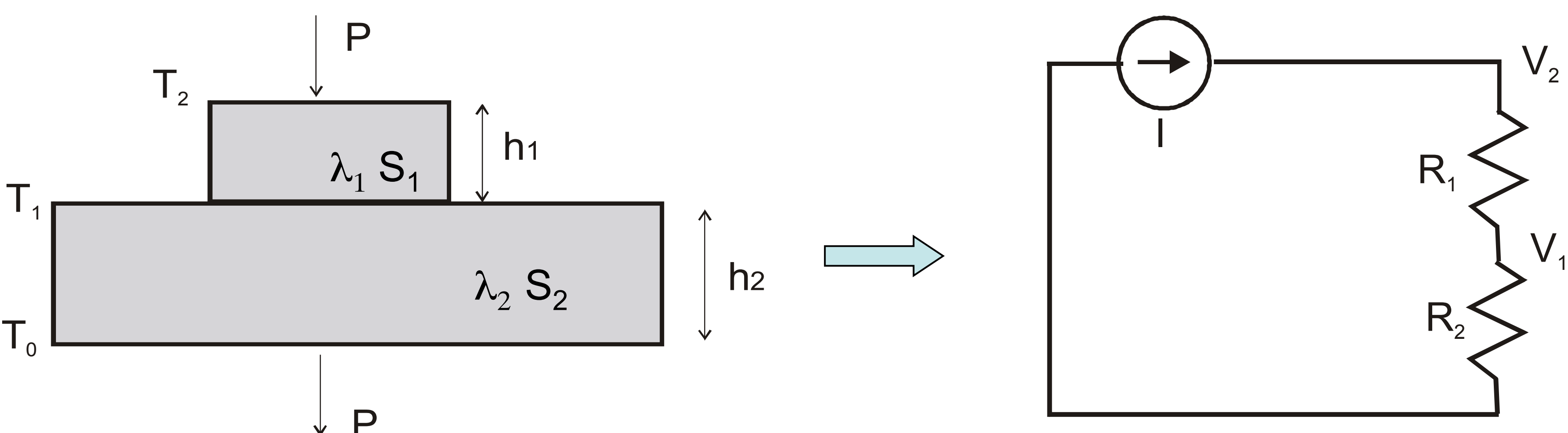
T_0

P

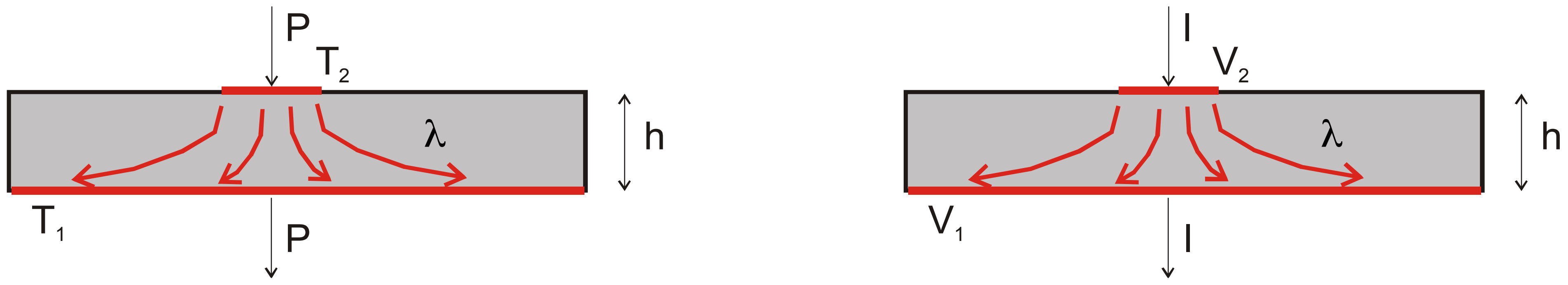
We can use an electrical equivalent for the heat transfer in steady state, to transform the thermal problem in an electrical network to be solved by usual means: :



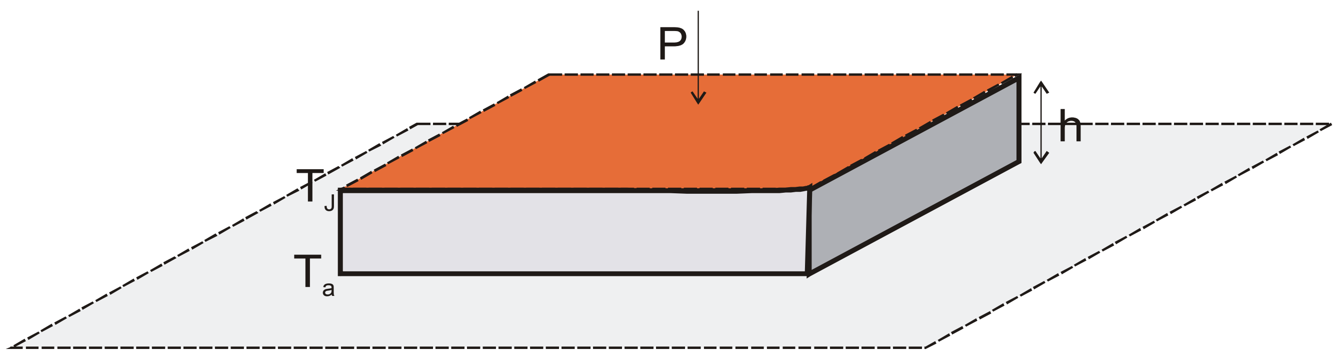
The electrical equivalent holds also for more bodies connected, and for heat flow in 2D and 3D cases, provided that for each body the value of R_{Ti} is evaluated with a 2D or 3D analysis.



The heat flow distribution in a 2D case is equivalent to the current flow distribution in the same geometry, by substituting the thermal conductivity λ with the electrical conductivity



First example for R_T :
Let's consider a silicon chip of surface S >> h (thickness), in contact with an ideal heat sink, that keep the inner chip surface at the ambient temperature T_a for any thermal power P.



If P_D is the electrical power dissipated on the active device in steady state (assuming the active device realized in the whole upper surface of the chip, with a device thickness W << h), then the thermal power P generated in the active area (red surface) is $P = P_D$ (all the electrical power is transferred to heat).

Then for the steady state heat transfer equation (1) we have:

$$T_J - T_a = R_T P; \qquad T_J > T_a$$

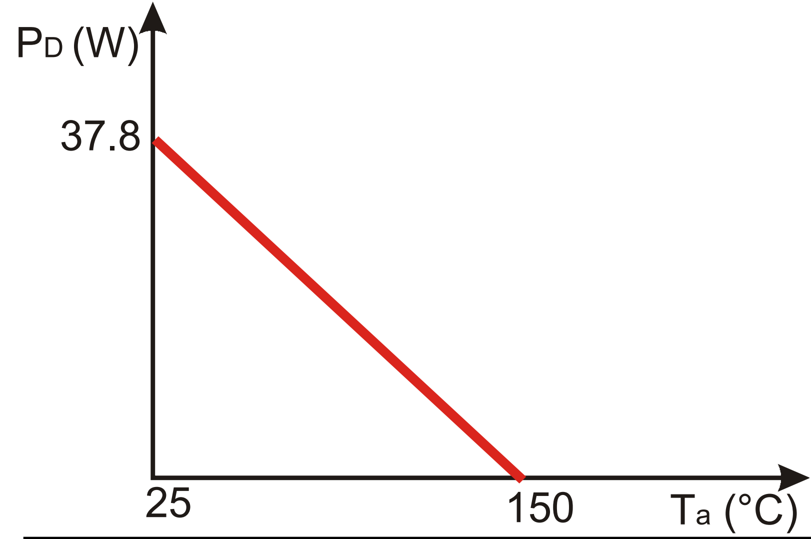
Assuming for our example:
h = 0.5 mm, S = 1 mm^2, λ = 1.5 W/cmK

we have: R_T = 3.3 K/W

$$R_T = \frac{h}{\lambda \cdot S}$$

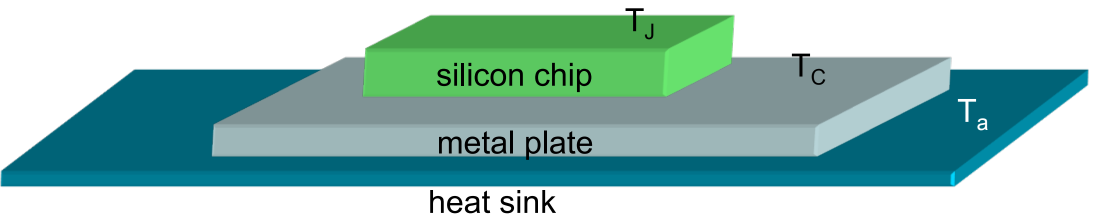
If a max temperature for the device junction T_{JMAX} = 150° is assumed, and an ambient temperature T_a = 25°, then the max power dissipation of the device is given by:

$$P_{DMAX} = \frac{T_{JMAX} - T_a}{R_T}; \qquad \text{per } R_T = 3.3\,\frac{K}{W} \qquad P_{DMAX} = 125/3.3 = 37.8\ \text{W}$$

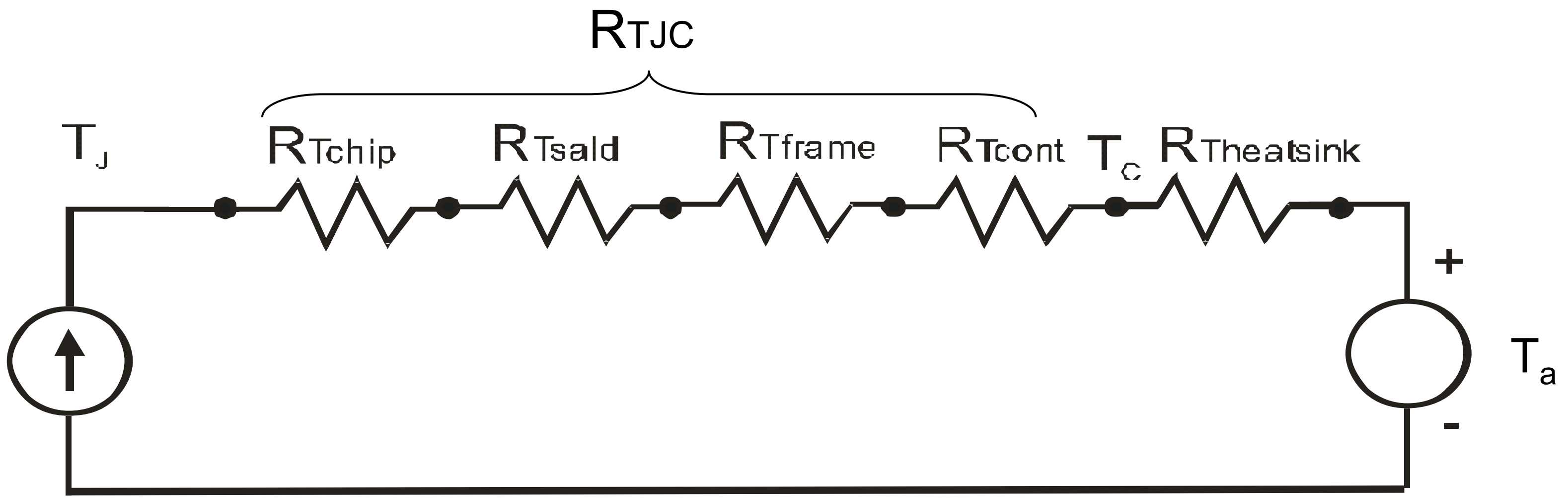


This relationship shows that the max power P_{DMAX} is dependent from the value of R_T , and the power derating of the device (figure on side) is linearly decreasing with the heat sink temperature (or the ambient temperature T_a).

Let's consider a more realistic case, of a silicon chip of area S_1 soldered on a metallic plate of area S_2 (the package frame), this latter connected (with another solder or glue) to an much larger heat sink (the plastic board or another base metal plate)

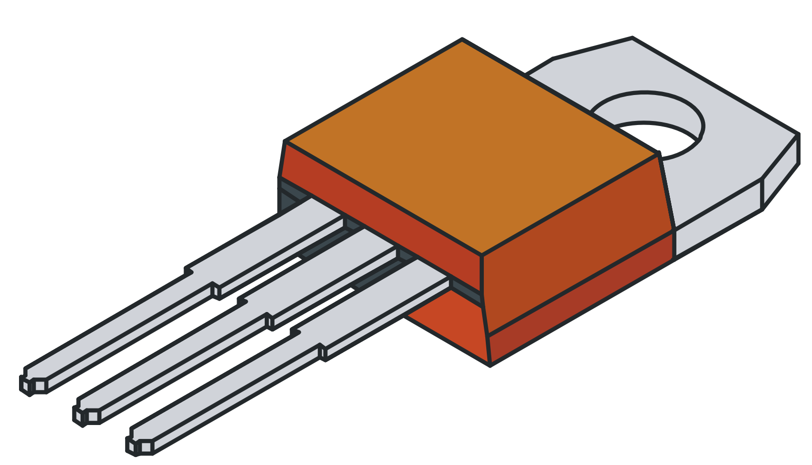


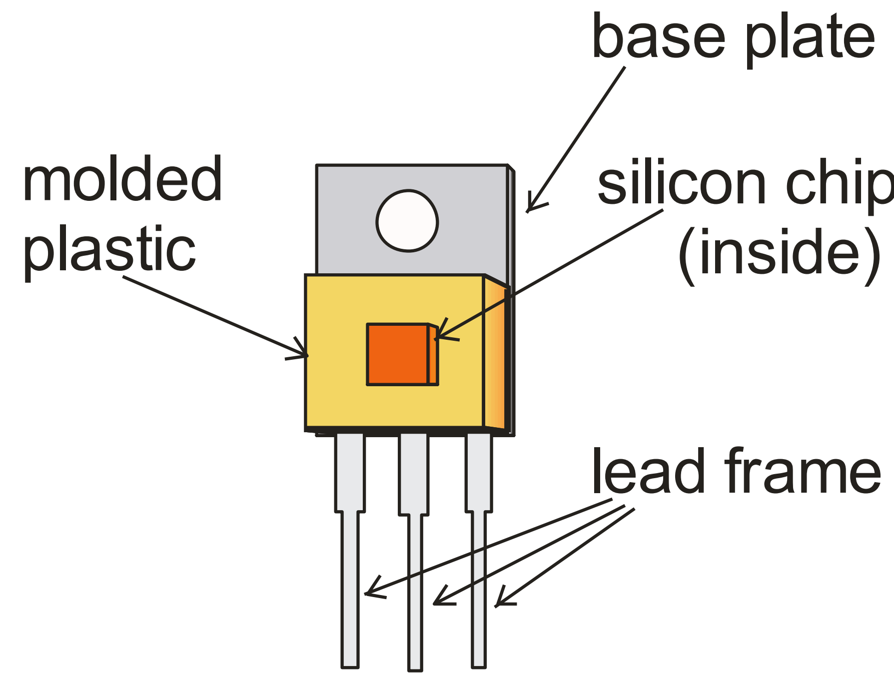
Considering again the electrical equivalent network, assuming for each material the corresponding R_T value, we have the following scheme, with an overall R_{TJC} for the temperature drop between the device (T_J) and the case (T_C), and a total R_{TJa} down to the ambient temperature

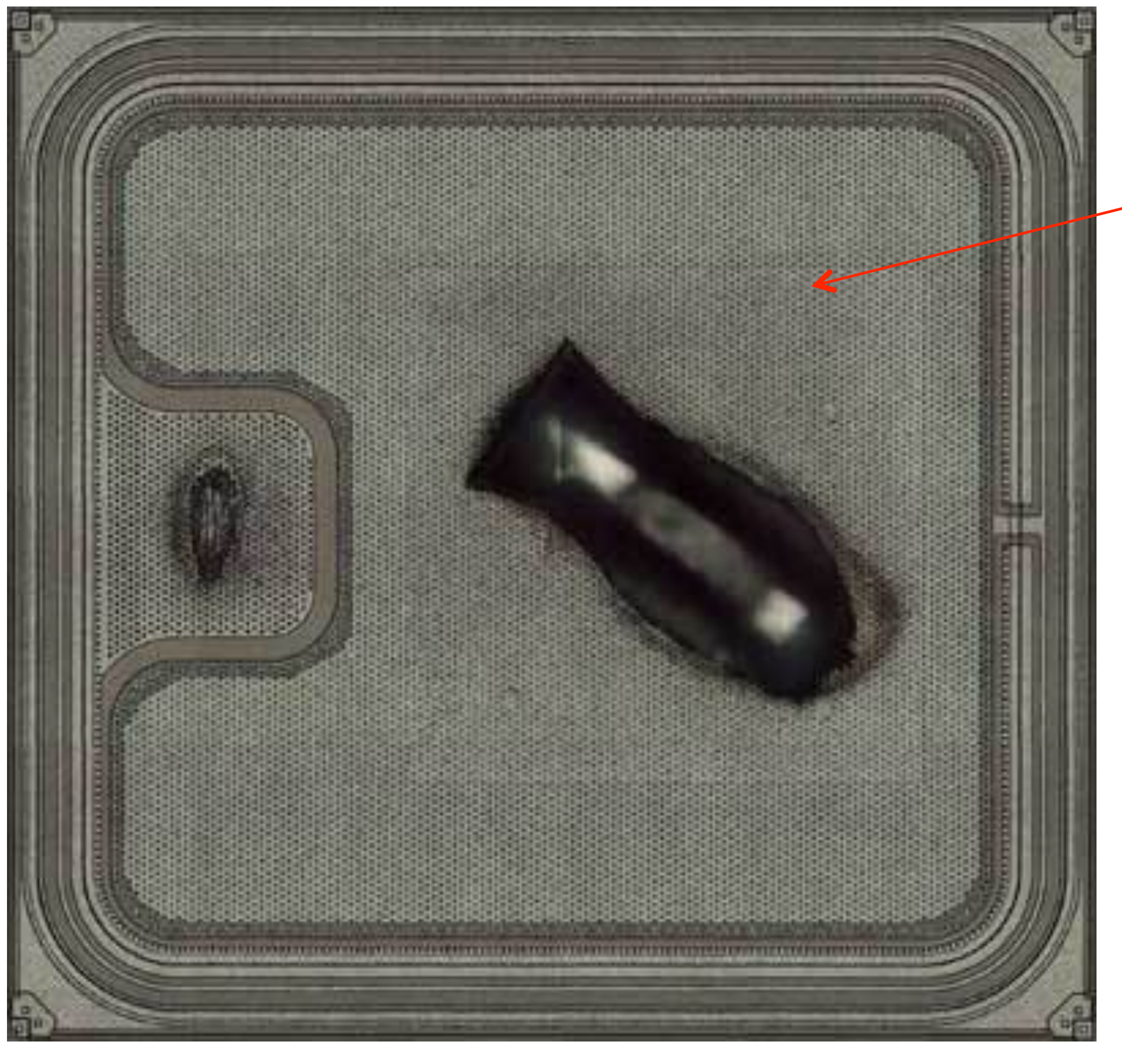


Typically, the device producers for each device and package define in the datasheets only the thermal resistance R_{TJC} i.e. the one between junction and case (the metal base plate for a basic package for medium power device, like the one sketched below).
The total R_{TJa} is obtained if one adds the thermal resistance between the case and the heatsink. This latter is largely dependent on the way the heat sink is made (plastic board, copper board, metal plate, finned aluminum block, water cooling or other ways)

typical TO-220 package used for power devices of several tens of W dissipation





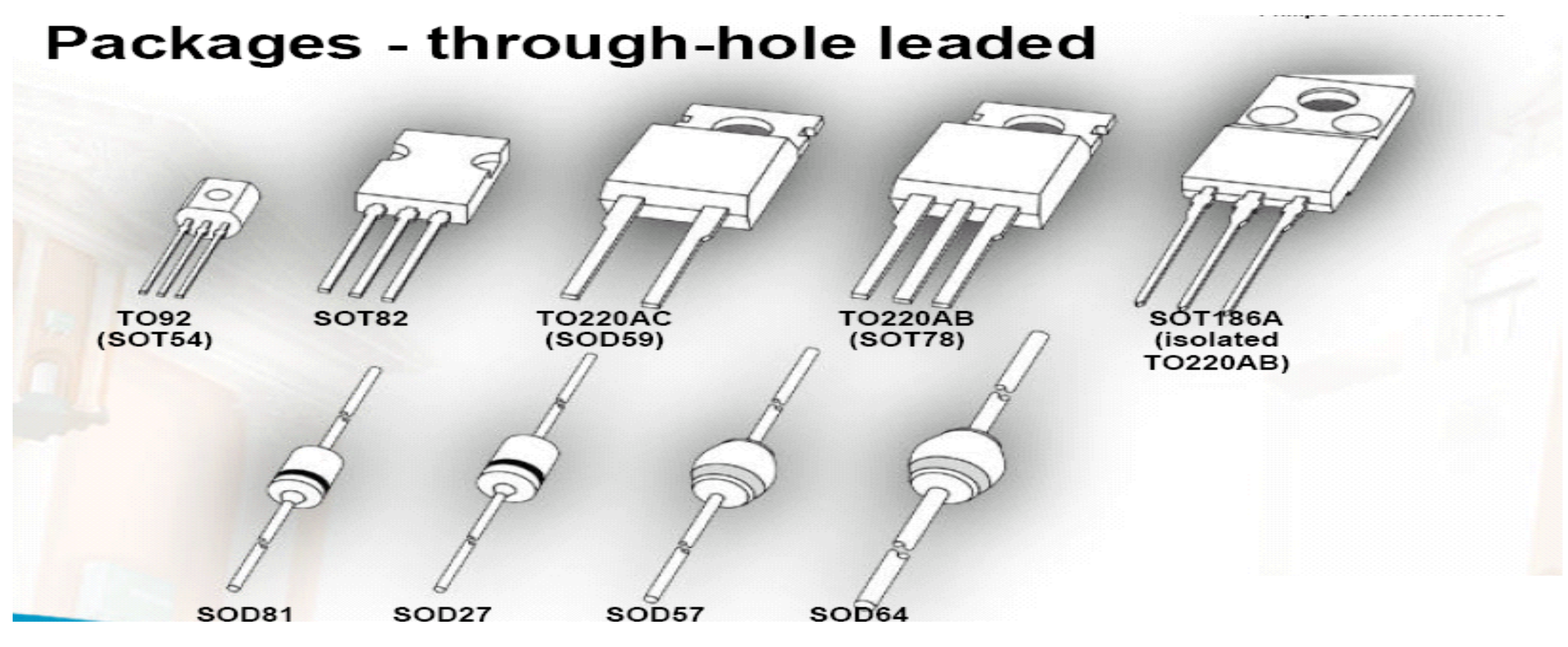


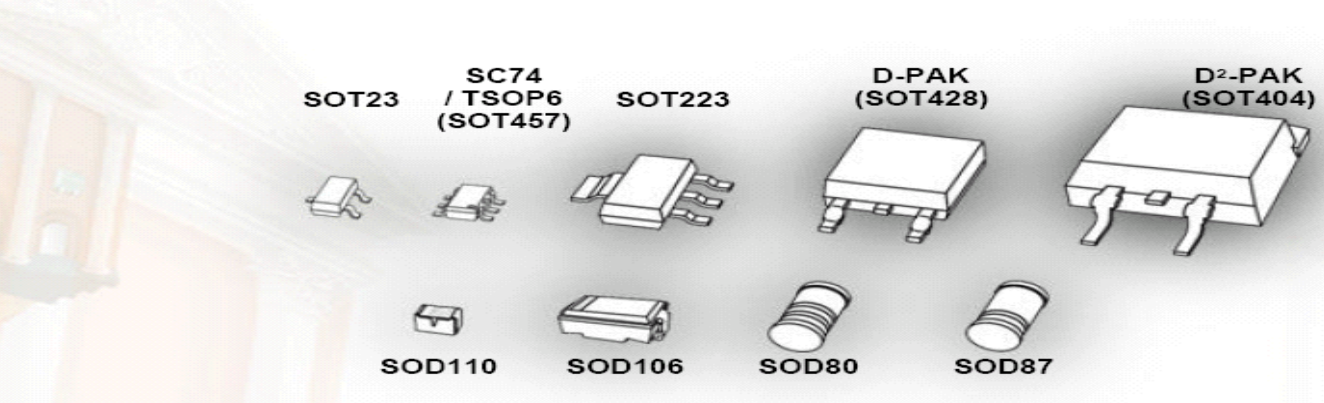
Aluminum on top

covered by polyimide passivant layer

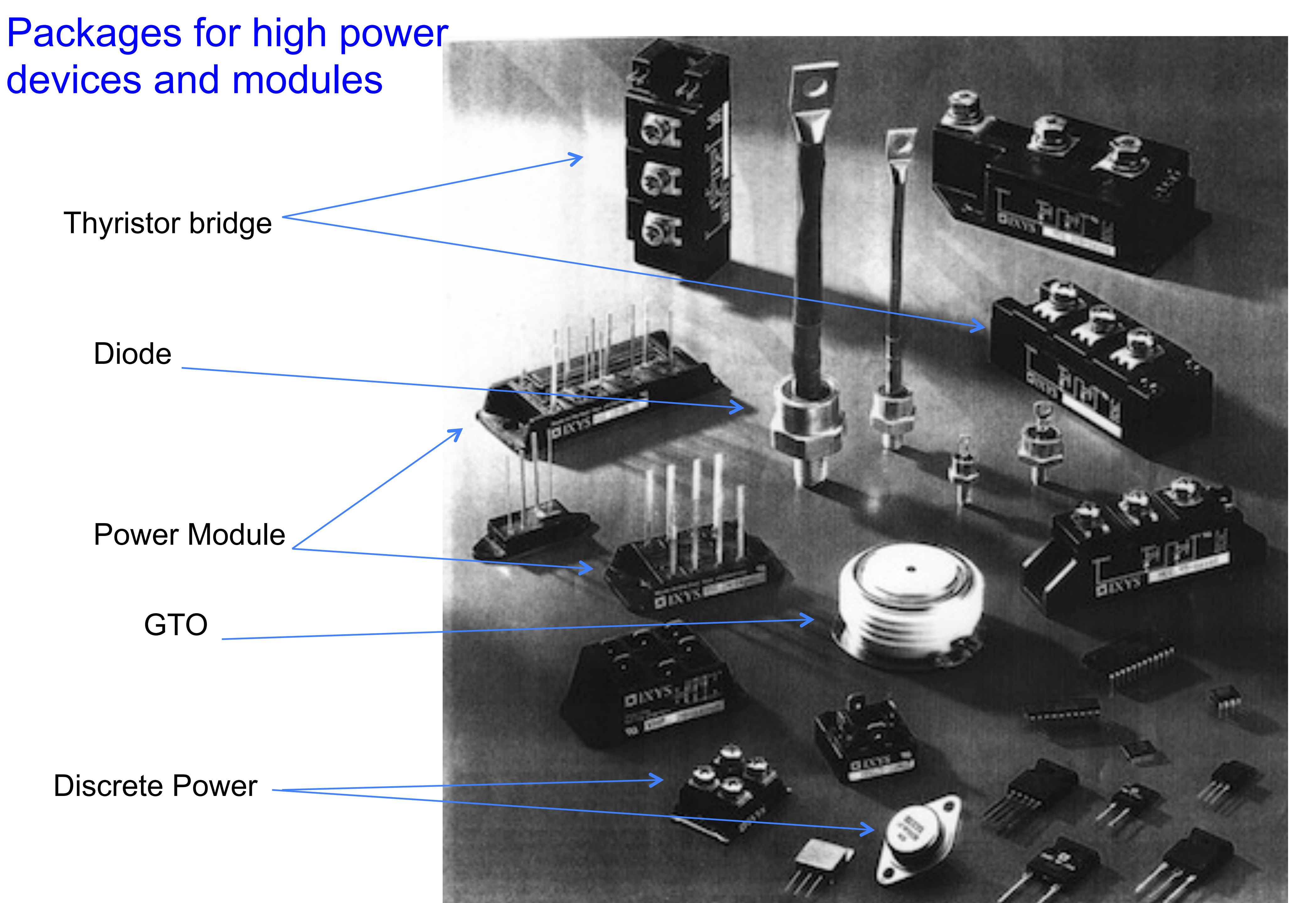
Image of a power MOS chip, of area 4.3mm^2, with the gate contact on the left and the remains of the aluminum 10-mil source-contact wire on the right.

Power packages for medium power devices



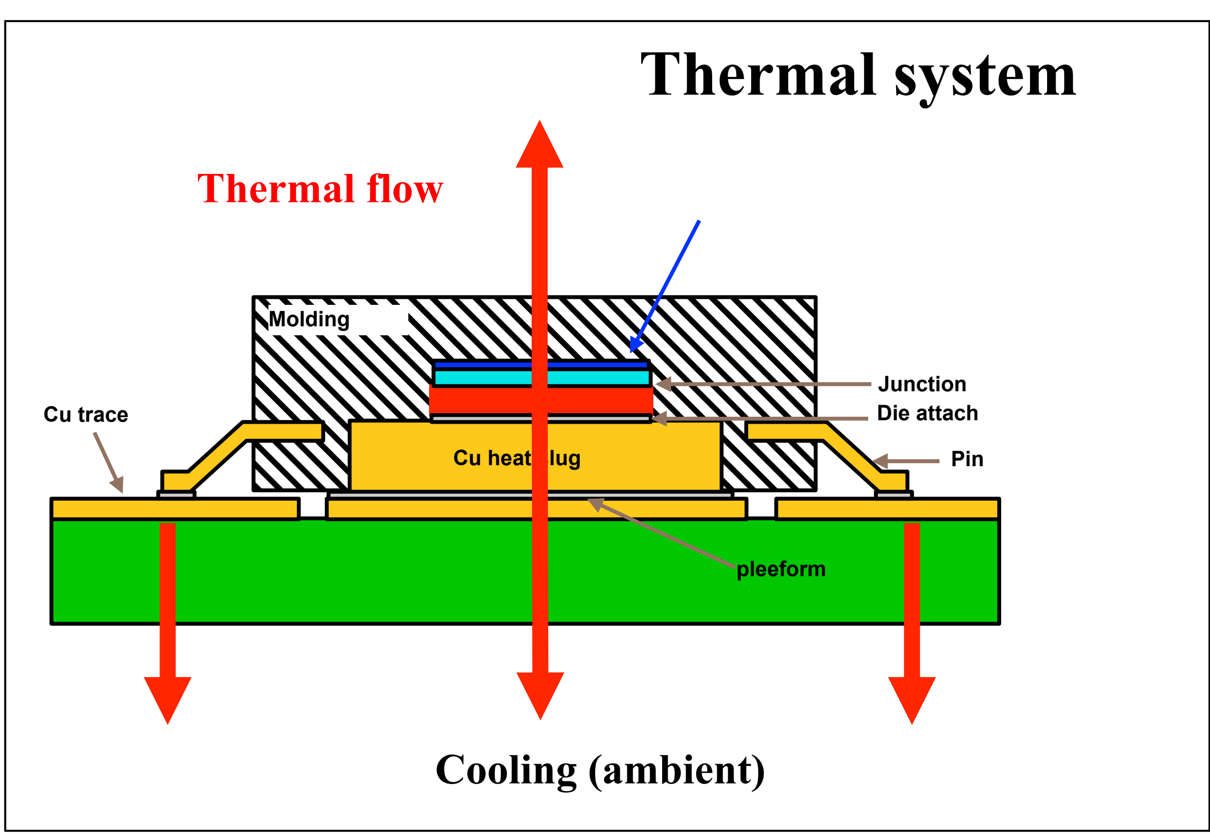


Packages for high power devices and modules



How to measure the junction temperature and the thermal resistance R_T?

The thermal system of a power device is complex and difficult to be analyzed by numerical simulations.
From experimental evaluation we can not use a thermocouple to detect the (internal) T_J : the area is too small and the package do not allow direct measurement.

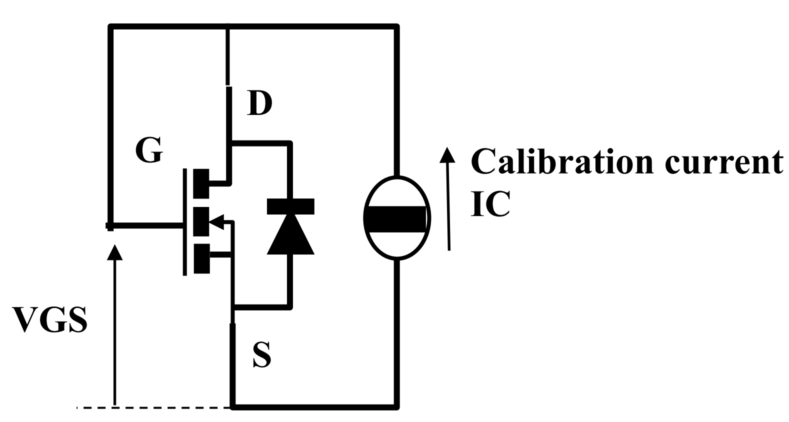


Example for a surface mount package

Tj measurement and calibration using device electrical characteristics

Device	A K (diode)	B C E (BJT)	G D S (MOSFET)	G C E (IGBT)
Parameter	V_{AK}	V_{BE}	V_{SD} V_{TH}	V_{TH}
Calibration circuit	A, K, I_F	B, C, E, I_F	G, D, S, I_F	G, C, E, I_D
Calibration condition	$V_{AK} = V_F + R_S * I_F$ IF $I_F << I_{NOM}$ → $V_{AK} = V_F$ (Same for Bipolar and PMOS		$V_{GS} = V_{TH} + G_{FS} * I_D$ IF $I_D << I_{NOM}$ → $V_{GS} = V_{TH}$ (Same for IGBT)	
Values used for Calibration	Those Values are only an indication to be checked case by case ΔV_F = -2 mV/°C @ IF = 250 µA		ΔV_{TH} = -6 mV/°C @ ID = 250 µA	

Tj measurement and calibration using device electrical characteristics
Example of the Power MOS

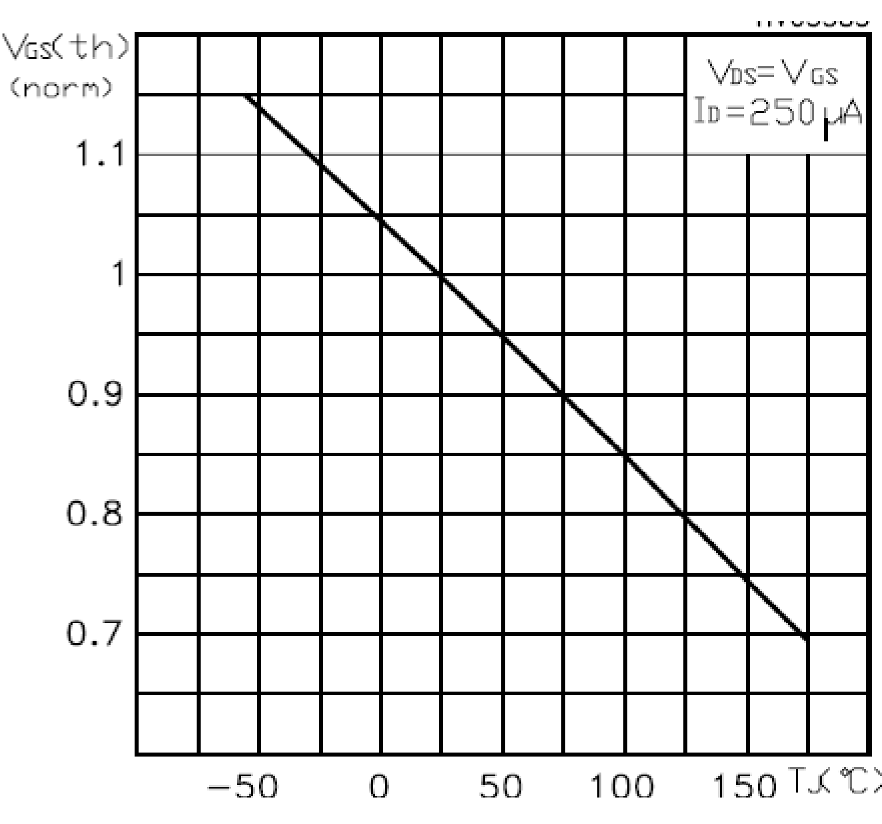


VGS threshold voltage can be used as a junction temperature sensor

$V_{GS} = V_{TH} + G_{FS} * I_D$

IF $I_D = IC \ll I_{NOM} \rightarrow G_{FS} * I_D = 0 \rightarrow V_{GS} = V_{TH}$

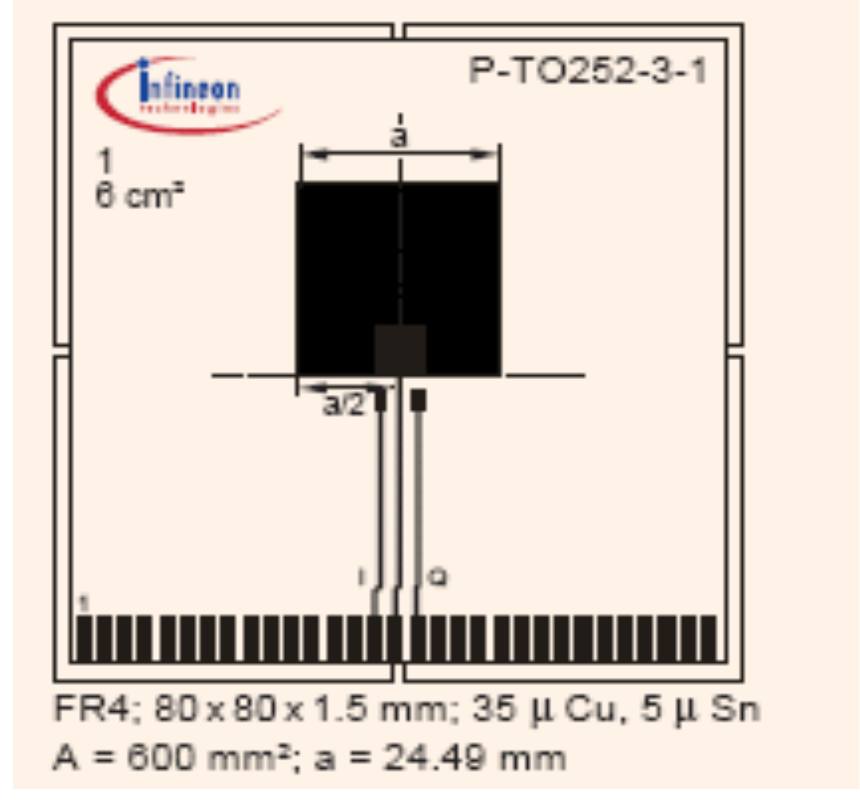
- Normalized gate threshold voltage versus temperature
- Device: STP80NF06: VTH typical @ 25°C = 3V



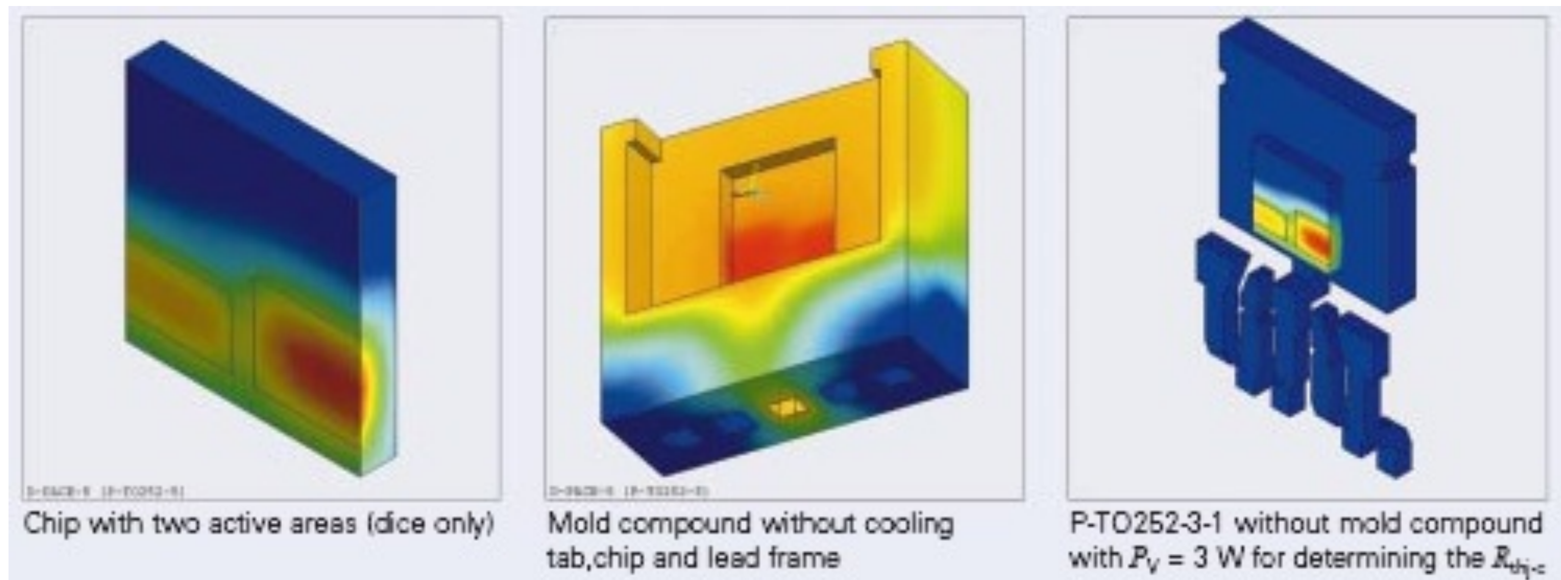
3D thermal analysis of a package in steady state

Here a 3D thermal analysis done with a F.E.M. numerical simulator, done for a TO252 package, mounted on a plastic board with copper coating, is reported, to give an idea the thermal resistance offered in realistic case.

P-TO252-3-1



The package is decomposed in his elementary parts (3D)

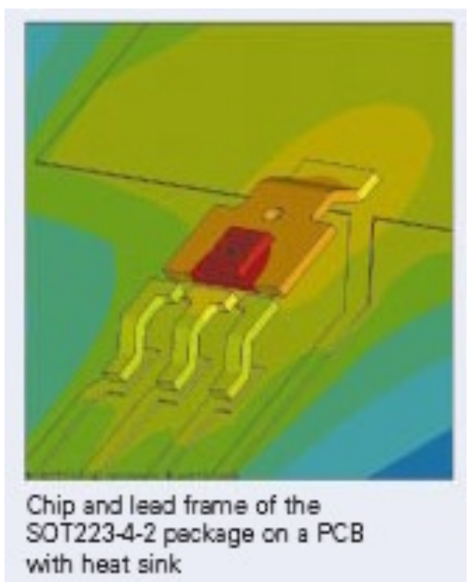


Chip with two active areas (dice only)

Mold compound without cooling tab,chip and lead frame

P-TO252-3-1 without mold compound with P_V = 3 W for determining the R_{thj-c}

(for each image the hottest areas are the red ones, the coldest in blue)



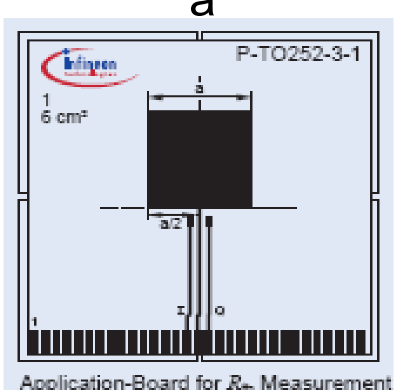
Chip and lead frame of the SOT223-4-2 package on a PCB with heat sink

two different copper design in the plastic board are investigated:

a) an area of 6 cm^2

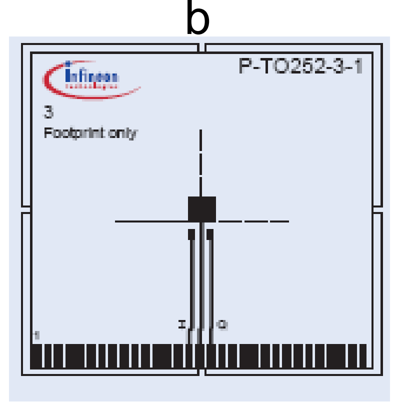
b) only a footprint area

a



Application-Board for R_{th} Measurement

b



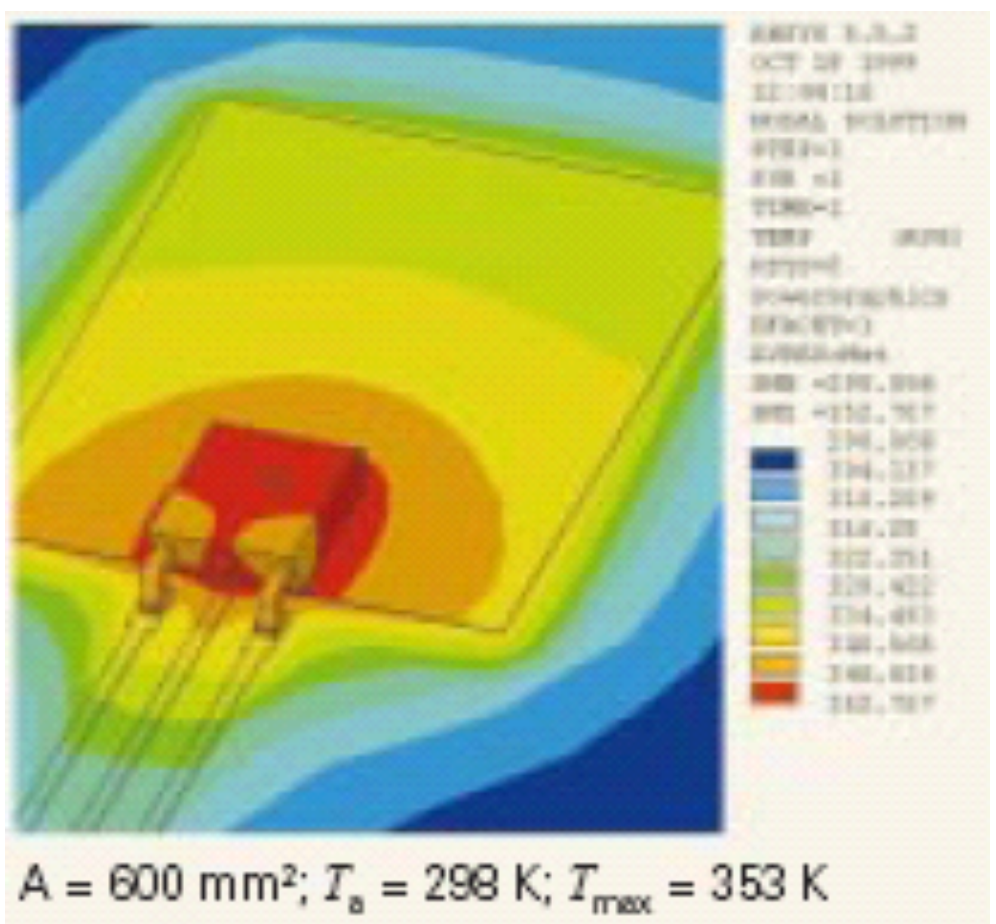
The results of the above 3D analysis are the following:

For a package with an R_{TJC} of about 1.8 C°/W one has for the case

(a) ΔTmax = 55 C° - total R_{TJa} = 54.7 C°/W

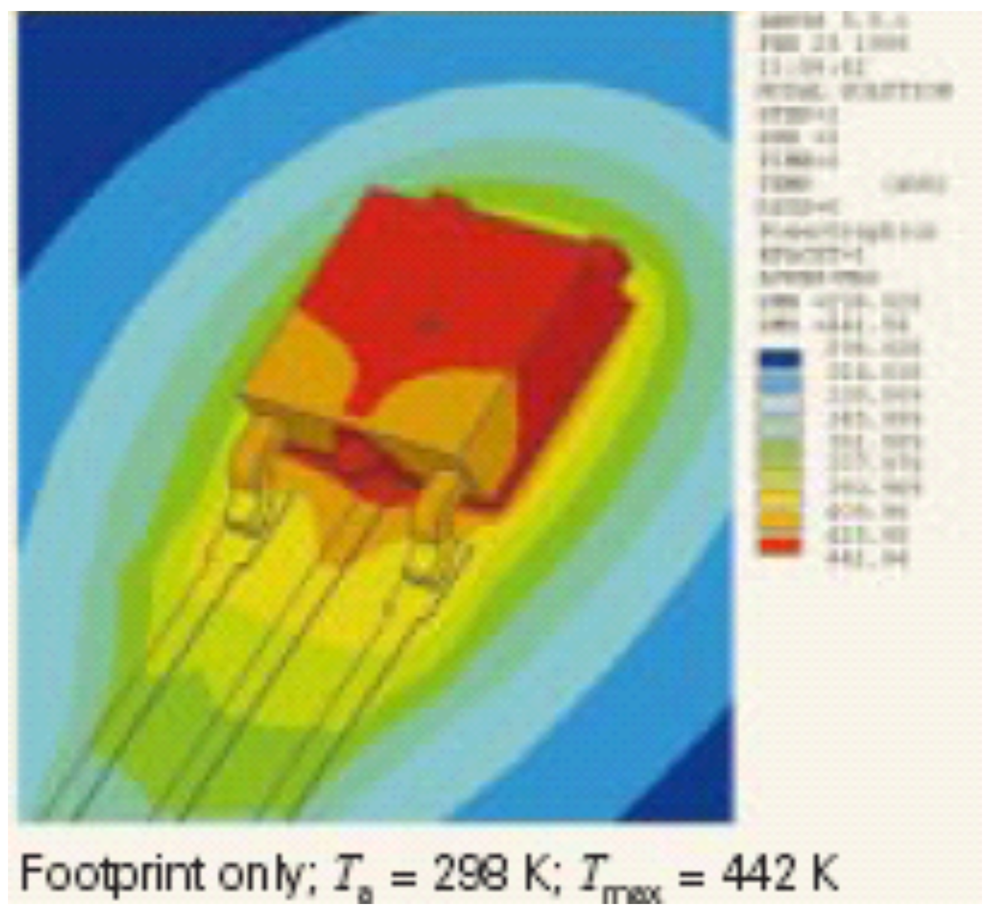
(b) ΔTmax = 144 C°/W - total R_{TJa} = 143.9 C°/W

(a)



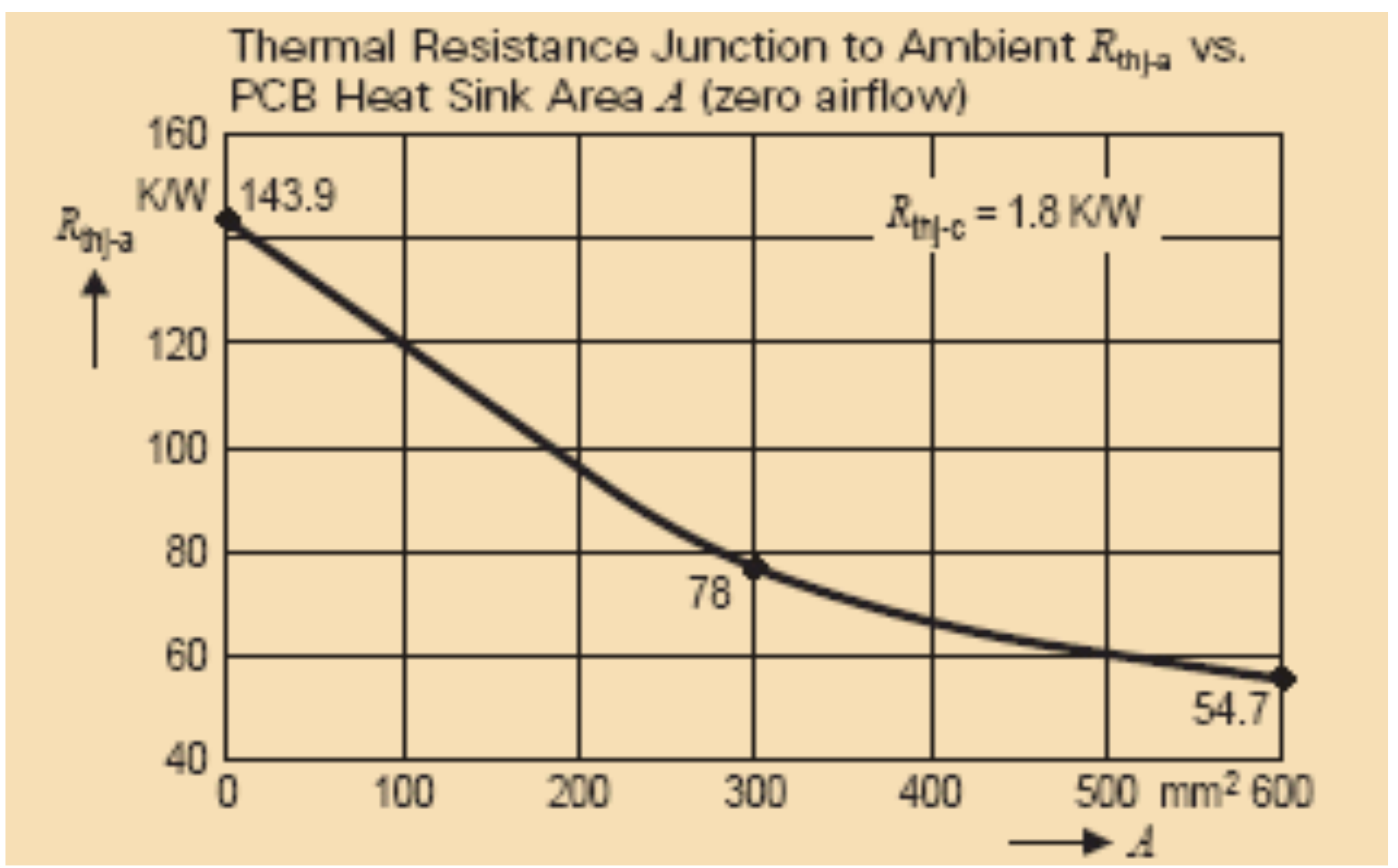
A = 600 mm²; T_a = 298 K; T_{max} = 353 K

(b)



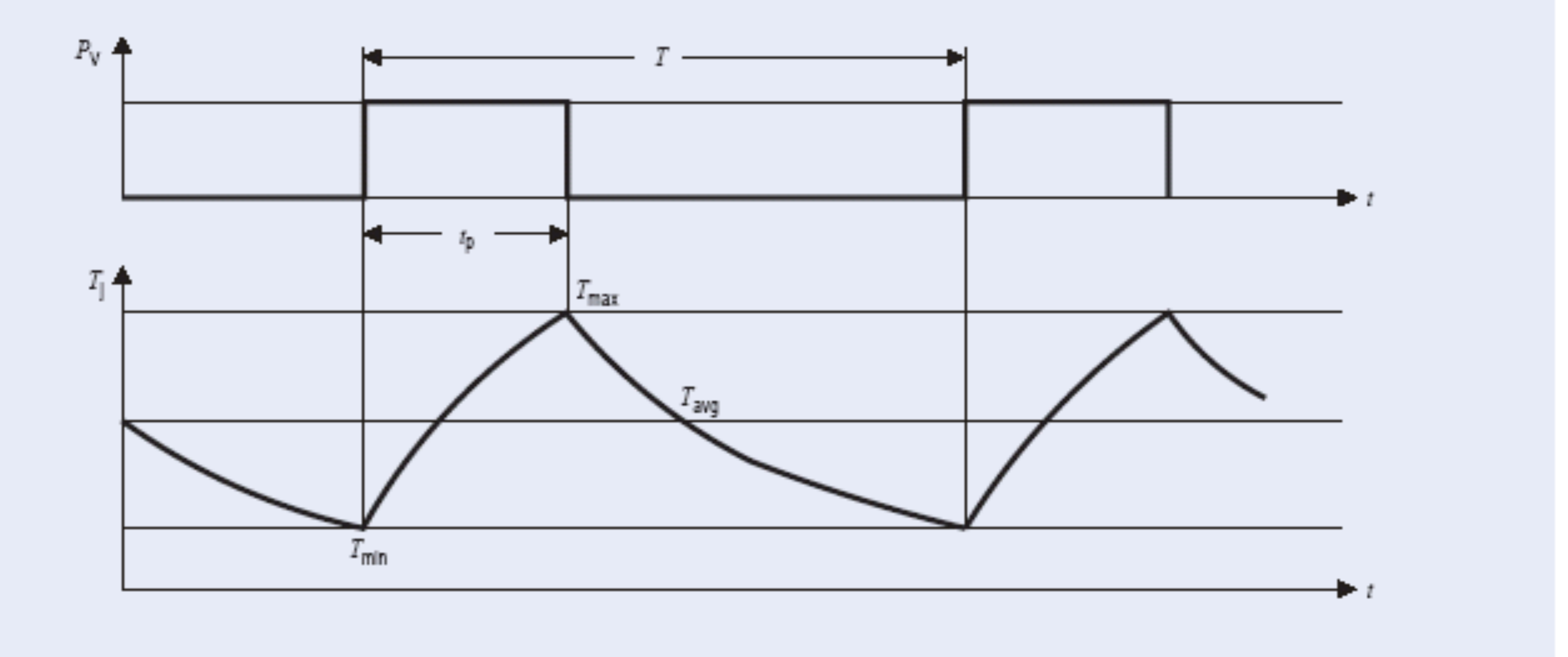
Footprint only; T_a = 298 K; T_{max} = 442 K

The value of R_{TJa} is largely dependent on the heat sink thermal resistance: for instance in the case analyzed, the R_T value is mostly dependent on the copper area left on the plastic board, as it can be seen by the plot below.



Transient thermal resistance

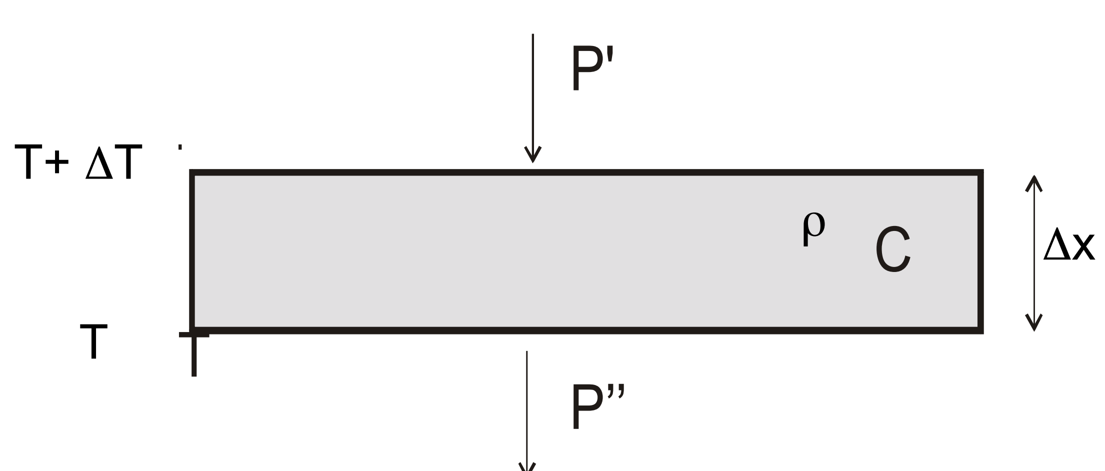
Up to now only steady state condition for the heat transfer have been considered. What happens if the electrical power is applied as short time pulses, as it can be the case in power applications?
In that case the temperature of the device area (where the electrical power is being applied) varies with time, and the max temperature reached during each power pulse depends both on the amount of power and of the time duration t_P of the power pulse, as well as on the pulse repetition period T.



Heat tranfer in transient

Considering again an one-dimensional case for the plate, if the heat flow P' entering from one surface is different from the one P" that exit from the other one, then there will some heat ΔQ increase or decrease in the unit time into the plate. This quantity that can be obtained by considering the specific heat C that is the heat to be given to the unity mass of material to increase its temperature of 1 °C.
The basic equation lies the heat variation ΔQ to the increase in temperature ΔT and to the specific heat and the density ρ of the material:

$$\Delta Q = S\Delta x \rho C \Delta T$$



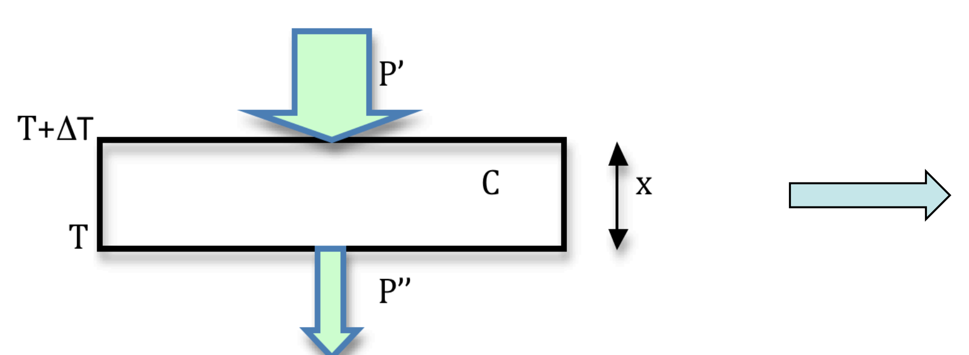
defining the volume $V = S\Delta x$
and the mass $m = V\rho$
one has:

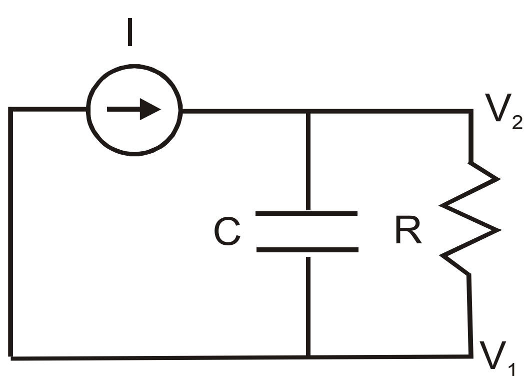
$$\Delta Q = mC\Delta T = C_T \Delta T$$

here C_T is defined as the thermal capacity of the plate of volume V and density ρ

Electrical equivalent network in transient

We have, for the electrical network equivalent :





Thermal | **electrical**

$$Q = \int_0^t P_C dt \quad \rightarrow \quad q = \int_0^t i dt$$

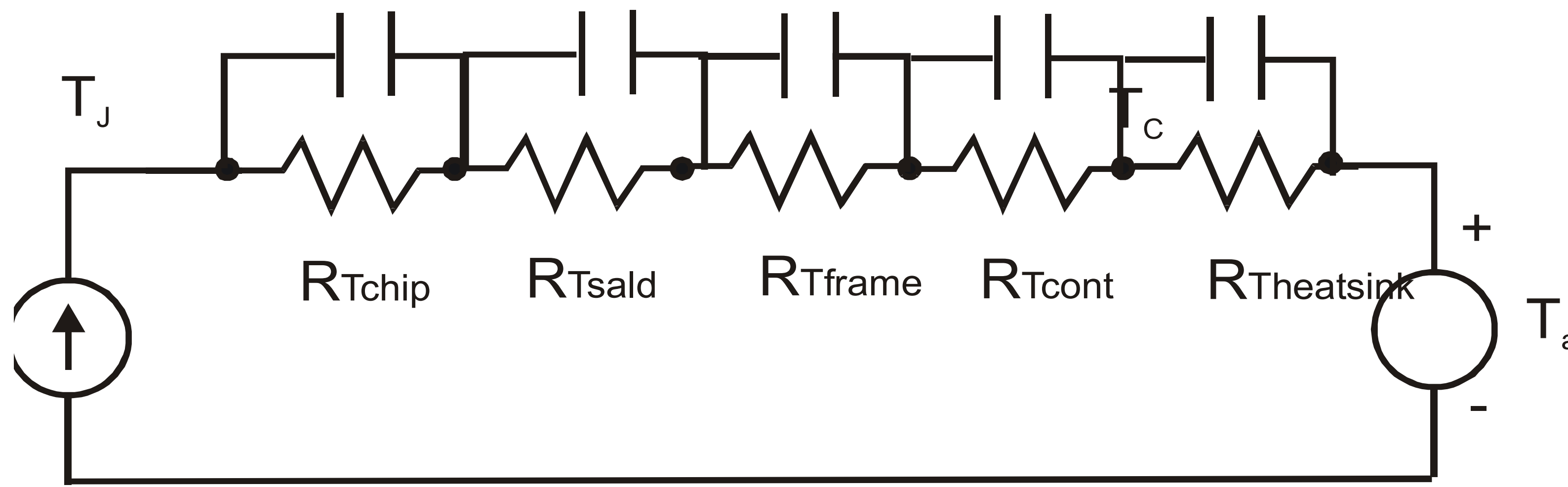
$$\Delta Q(t) = C_T \Delta T(t) \quad \rightarrow \quad \Delta q(t) = C \Delta V(t)$$

$$R_T(t) \equiv Z_T(t) = \frac{\Delta T(t)}{P(t)} \quad \rightarrow \quad Z_T(t) = \frac{\Delta V(t)}{I(t)}$$

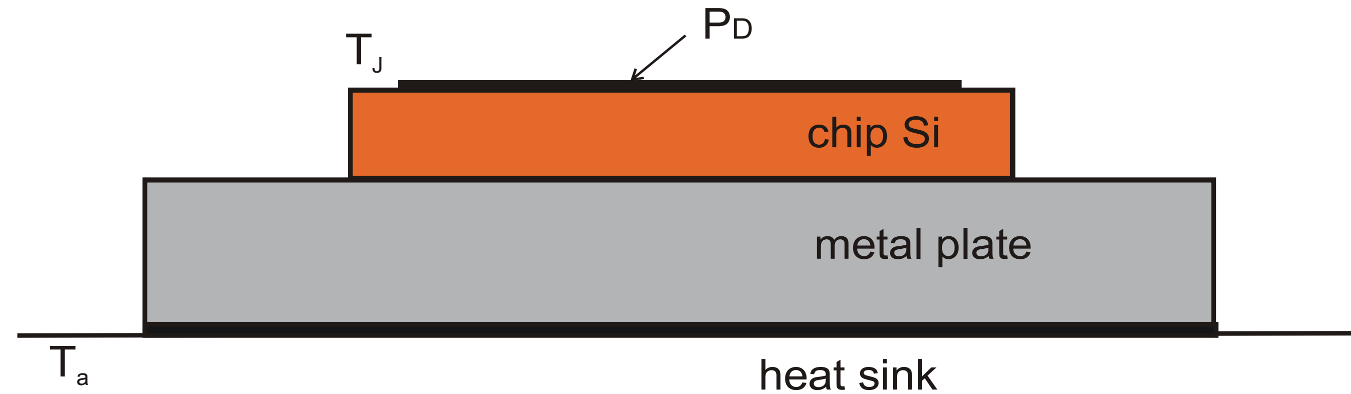
THERMAL IMPEDANCE Z_T

The transient thermal resistance (or transient thermal impedance) Z_T of the device is then defined as the ratio between the transient increase in temperature of the junction and the power applied during the same time interval.

If the heat flows across more bodies, then the equivalent electrical network is represented by a series of RC meshes. For the case of chip+metal plate+heatsink we have:



Let's evaluate as an example the equivalent R_T and C_T values for a simple structure: silicon chip + metal plate



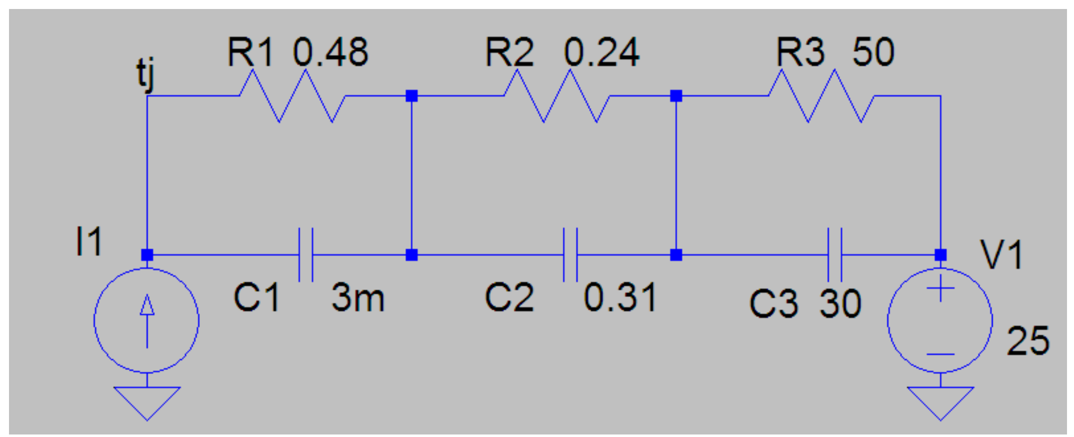
Chip

h 360 μm 0.036 cm
S 5 mm² $5 10^{-2}$ cm²
λ 1.5 W/cm .K
R_T 0.48 °C/W
ρ 2.33 g/cm³
M 4.2 10^{-3} g
C_S 0.7 Ws/gK
C_T 3 10^{-3} Ws/K

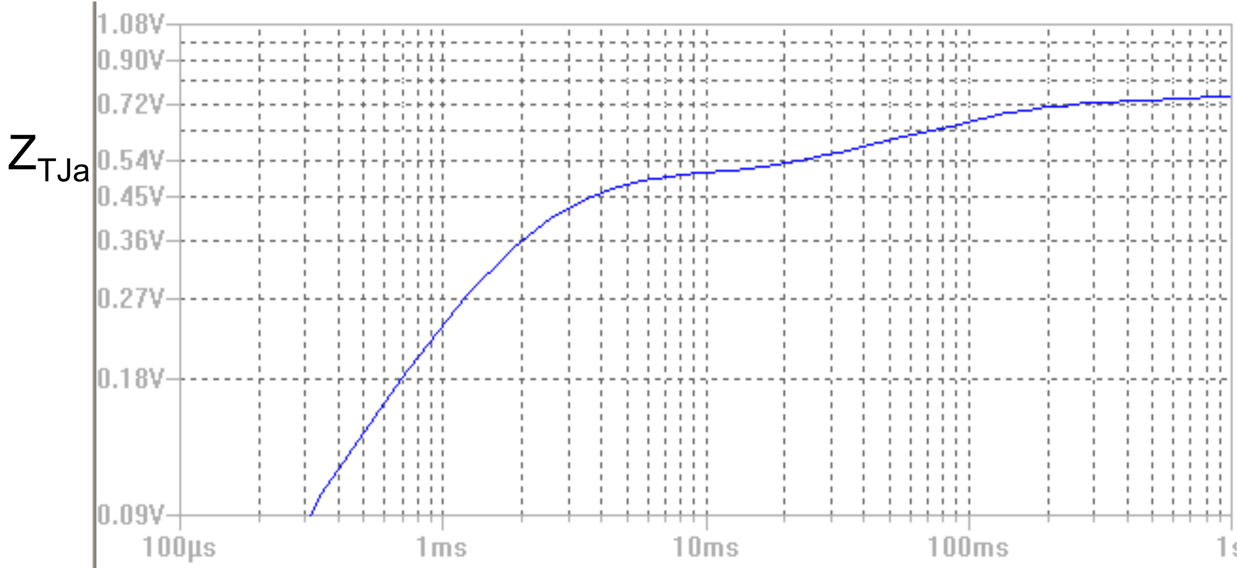
Copper metal plate

h 1.27 mm 0.127 cm
S 14 mm² $14 10^{-2}$ cm²
λ 3.84 W/cm .K
R_T 0.24 °C/W
ρ 8.93 g/cm³
m 0.8 g
C_S 0.385 Ws/gK
C_T 0.31 Ws/K

Based on the above values (and adding the values R3, C3 for a typical heat sink) we have the following electrical network, where one must evaluate the V(tj) value vs time for a step I1 input of 1A

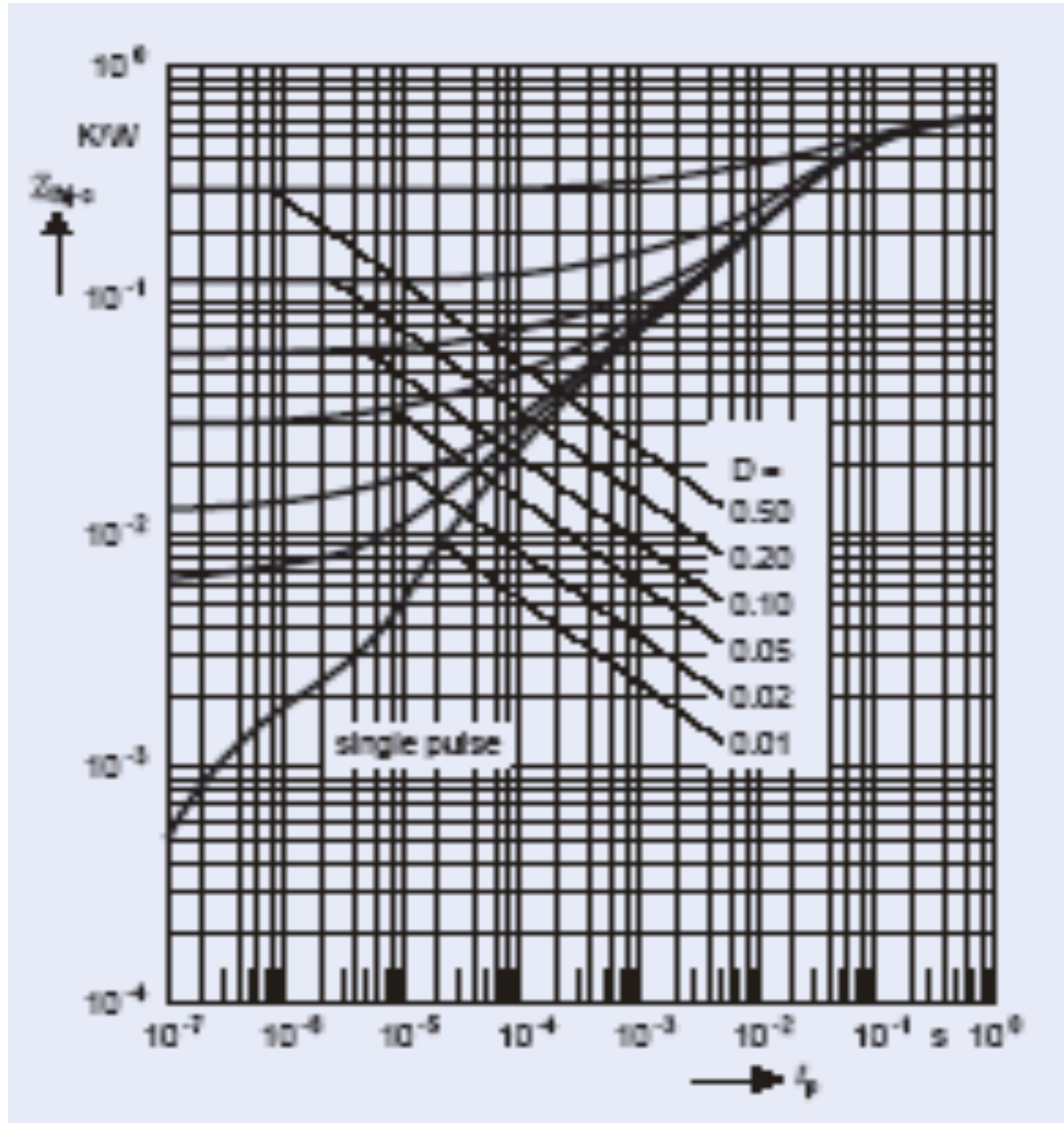


in this network, Z_{TJa} corresponds to:
V(tj) – V1
where V1 is 25 (corresponding to Ta - ambient temperature)



The result is plotted in log scale for both Z and time, and it is clearly shown the effect of the 3 time constants: first one depending on Si chip, second on metal plate, and third on heat sink (that will mainly contribute to the steady state R_T)

Typical Zth-c plot for a power device in a T0-220 package



This plot reports the values of the thermal impedance Z_T as a function of the time duration of the power pulse applied, and for different duty cycles D.

For the single pulse the thermal impedance tend to vanish for very low time pulses.
For the case of a periodic sequence of power pulses, the value of duty cycle D determines the low time value of $Z_T(t)$, because for times less than the lower time constant the device sees only the average power applied, that is is DxP.

Power ratings for pulse power (pulse S.O.A)

Assuming a pulse power given to the device, from the basic equation, due to the decrease of Z_T for short times, we have a max power in pulse operation larger than the one in steady state case:

$$P_{MAX}(t) = \frac{T_{JMAX} - T_a}{Z_T(t)}$$

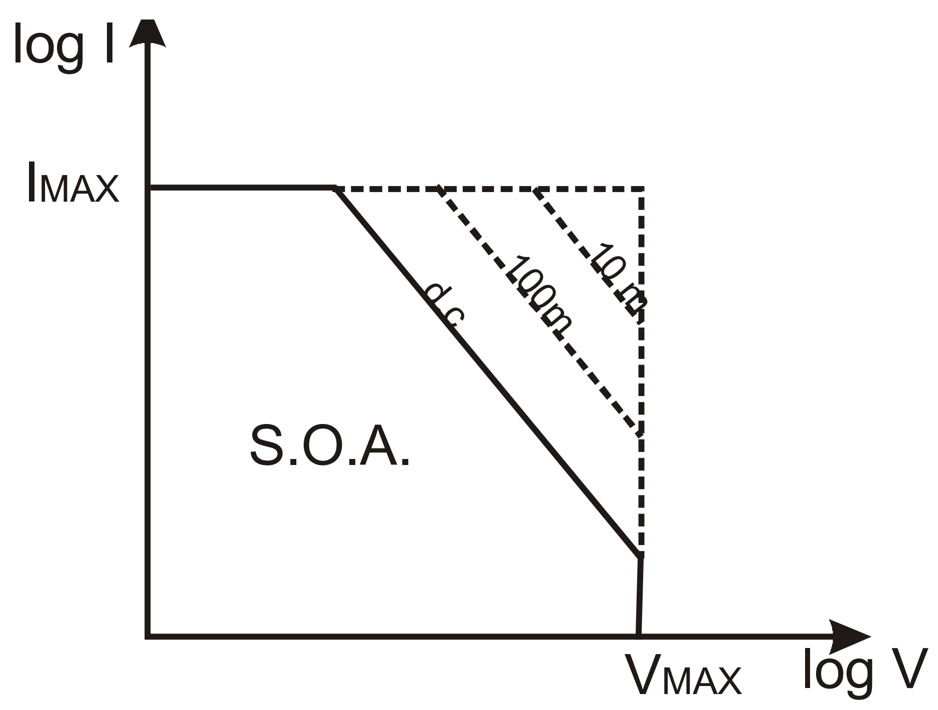
Assuming as an example:
Single power pulse with duration t_O = 100 μs
$Z_T(t_O)$ = 0.05 K/W
Max junction temperature = 150 °C
Ta = 25 °C

we have a max power dissipation of:

$$P_{DMAX}(t_O) = \frac{T_{JMAX} - T_a}{Z_T(t_O)}$$

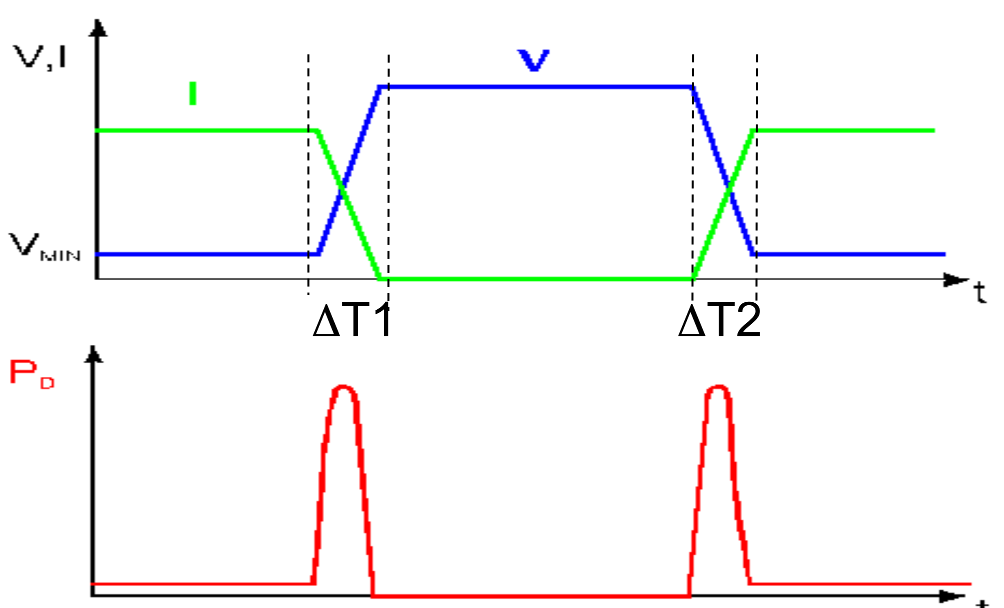
$$Z_T(t_O) = 0.05\frac{K}{W}$$

$$P_{DMAX}(t_O) = 2500 \;\; W$$



Dynamic power dissipation

As pointed out at the beginning of this section, there is a power dissipation in the device also during the switching of the device from the off state to on state and viceversa.

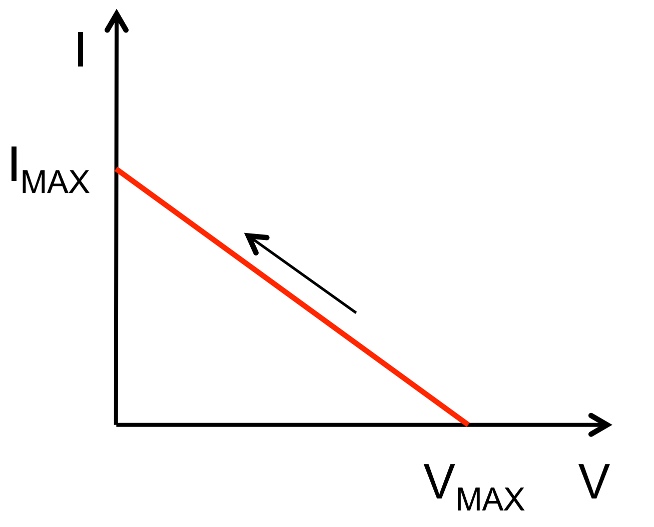


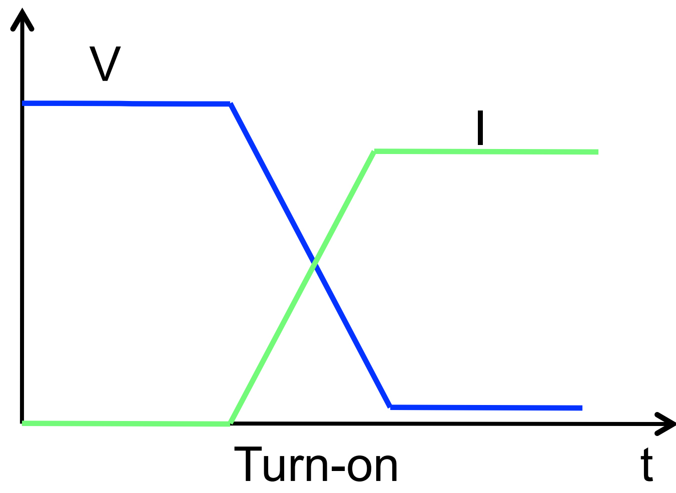
Indicating as ΔT1 the switching time from ON state to OFF state , and ΔT2 the one from OFF to ON, the dynamic power dissipation in one cycle (average power dissipation) is given by the general relation:

$$P_{Dd(av)} = \frac{1}{T} \int_{\Delta T1+\Delta T2} p_{Dd} = \frac{1}{T} \int_{\Delta T1+\Delta T2} i(t)v(t)dt$$

For all devices, the max values of p_{Dd} are usually much higher than the p_{DS} ones; then to reduce the average power dissipation P_{Dd} is it necessary to have switching times ΔT much less than the period T: this is usually the case in class D operation for the switching devices.

Assuming for a simple case that both the current and voltage vary linearly with time at the same time (this is the case for resistive load for the active device, where the current and voltage vary with the move of the operation point along the load line), the peak power dissipation P_{DdMAX} in each commutation is: $P_{DdMAX} = (I_{MAX}*V_{MAX})/4$, a value much larger that the istantaneous d.c. power dissipation in the ON state = $I_{MAX}*V_{ON}$.

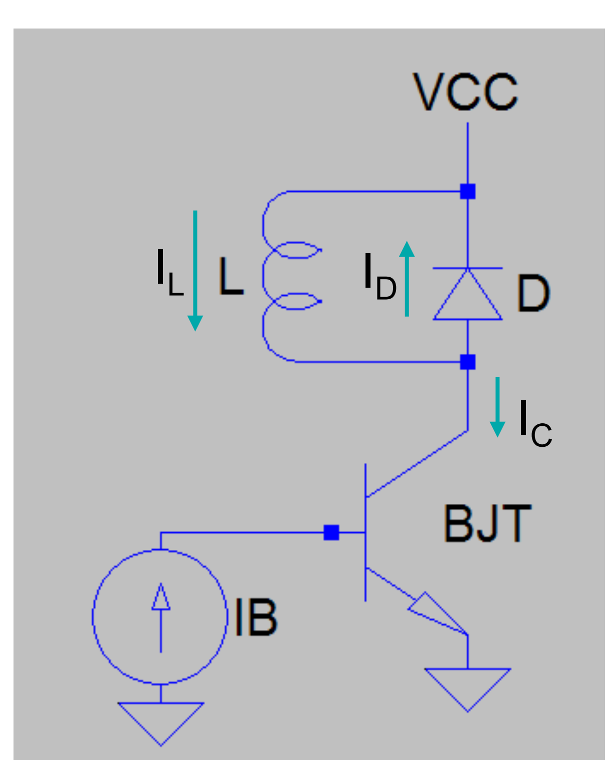




However, the switching time for most of the devices, is relatively short, from tens of nanoseconds to a few microseconds, so the power limits given by the pulse S.O.A. are the full square SOA, as indicated in the pulse SOA limits, and the switching power can be handled by the device within its operating limits, provided that I_{MAX} and V_{MAX} are contained in the device ratings.

Power losses with inductive load switching

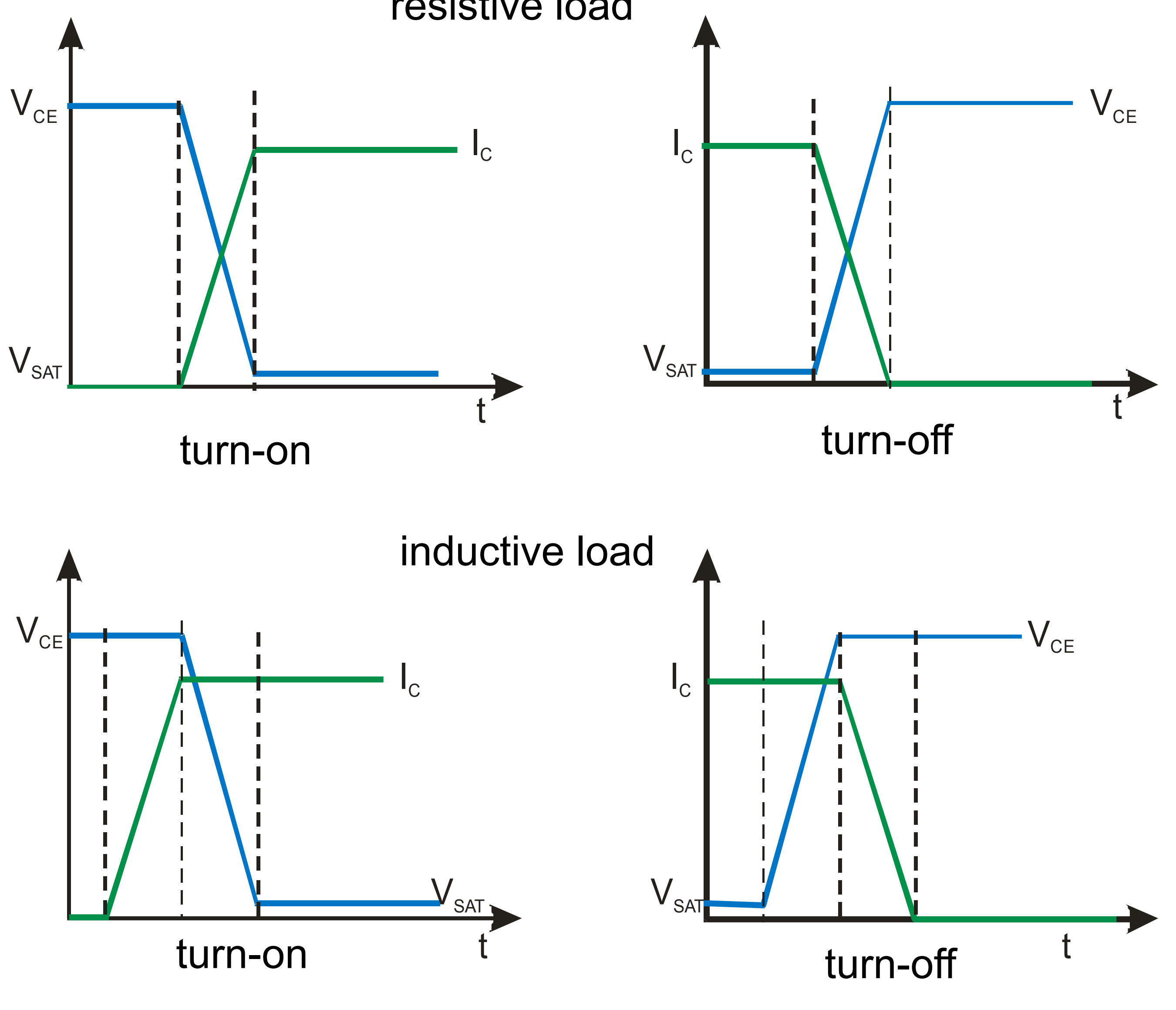
What happen of the dynamic power losses in the active device during turn-on and turn-off if the load is an inductive one (we know that is the typical load for power circuits)?
With reference to the simplified circuit in figure (assuming as example a BJT as the active device), with an inductive load with a fly-back diode (to allow the I_L current flow when the device is in off state), assuming a constant current I_L into the inductance during the turn-on and turn-off transients, we can do the following analysis.



a) turn-on: before transient the device is in OFF condition (I_C = 0) and all the current I_L is flowing into the diode D; this latter is in ON with a $V_{ON} \cong$ 1V. During turn-on the current I_C start to increase, but the diode D is still in ON state until the current I_C becomes equal to I_L, and the voltage V_{CE} start to decrease only at this time (and the diode is in OFF state with a reverse bias across it)

b) turn-off: before transient the device is ON and all the current I_L flows into the collector; after the storage time the collector voltage start to increase, but the current I_C is still equal to I_L because the diode is still in OFF state until the V_{CE} increases up to the V_{CC} value.
Only at that time the diode goes in ON state with a forward current I_D and the current I_C start to decrease. The difference I_L-I_C is the diode current I_D and after turn-off $I_D = I_L$.

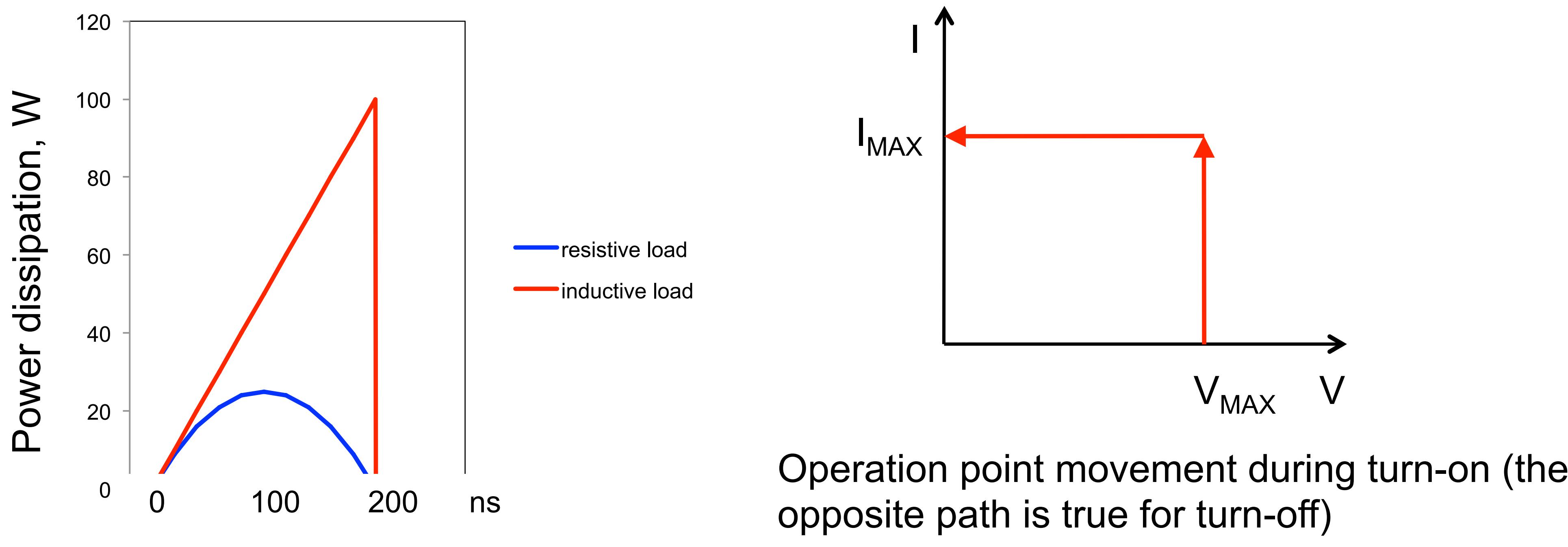
Comparison between resistive and inductive load switching



In this figure the dynamics of resistive and inductive switching are ideally sketched according to the analysis done previously (these results are equally appliable to the MOS case).

We can see that in the case of inductive switching the power losses are larger than for resistive switching, because in the latter case, during the transient of one variable the other remains constant at the max value (In the above analysis the diode is assumed ideal, and no parasitic effects are considered).

A comparison between dynamic power losses with resistive or inductive loads is sketched in the figure below, where the instantaneous power dissipation for the two cases are plotted during a turn-on phase of 200 ns, for the case of I_{MAX} = 10 A, V_{MAX} = 10V : for the case of inductive load, the average power dissipation P_{Dd} is more than three times larger than for the resistive load.



Operation point movement during turn-on (the opposite path is true for turn-off)

Even in that case, the switching power can be handled by the device, provided that I_{MAX} and V_{MAX} are contained in the device ratings, because the operation point will move along the limits of the square SOA (we will see later on that some added effects due to parasitic circuit components will risk to overcome the square SOA limits)