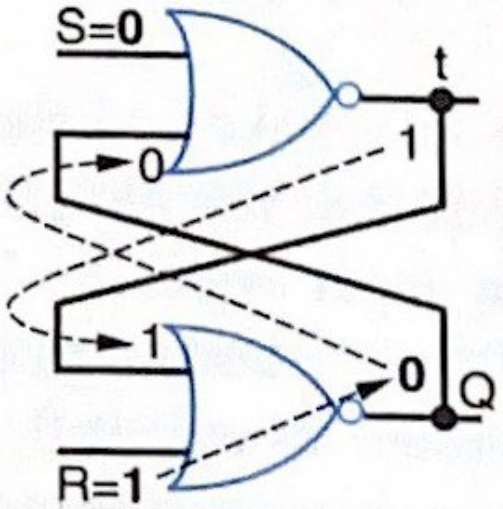
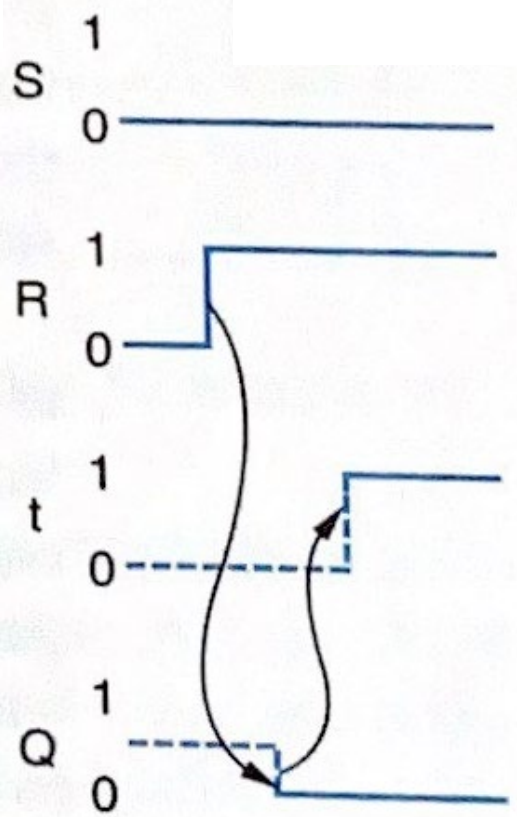
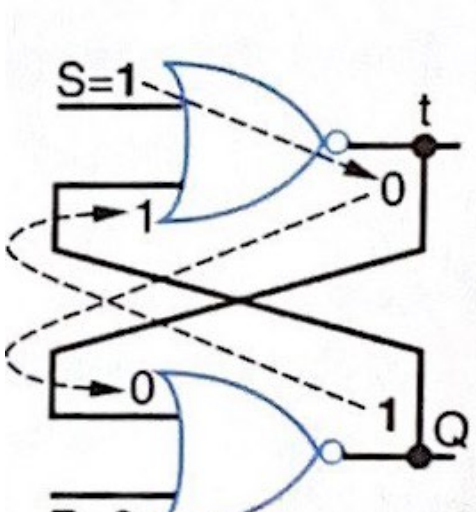
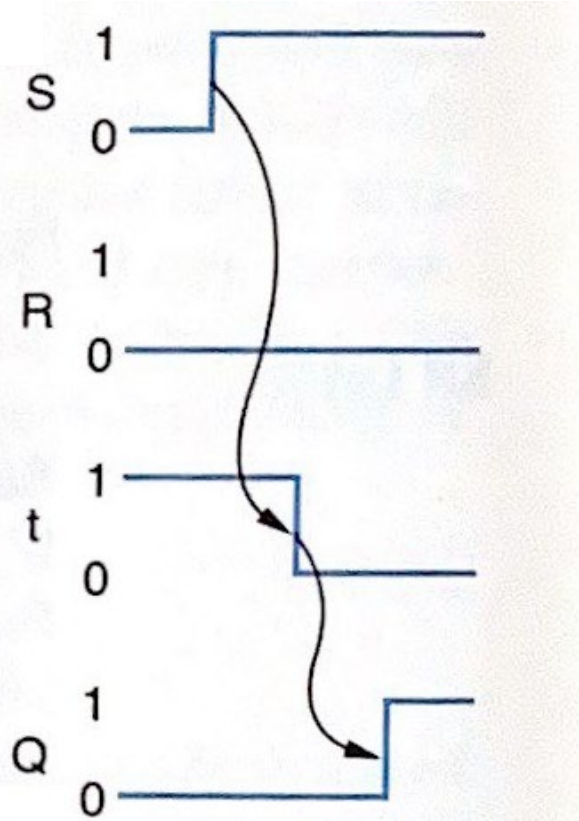
9- Latches & Flip-Flops

Set & Rst

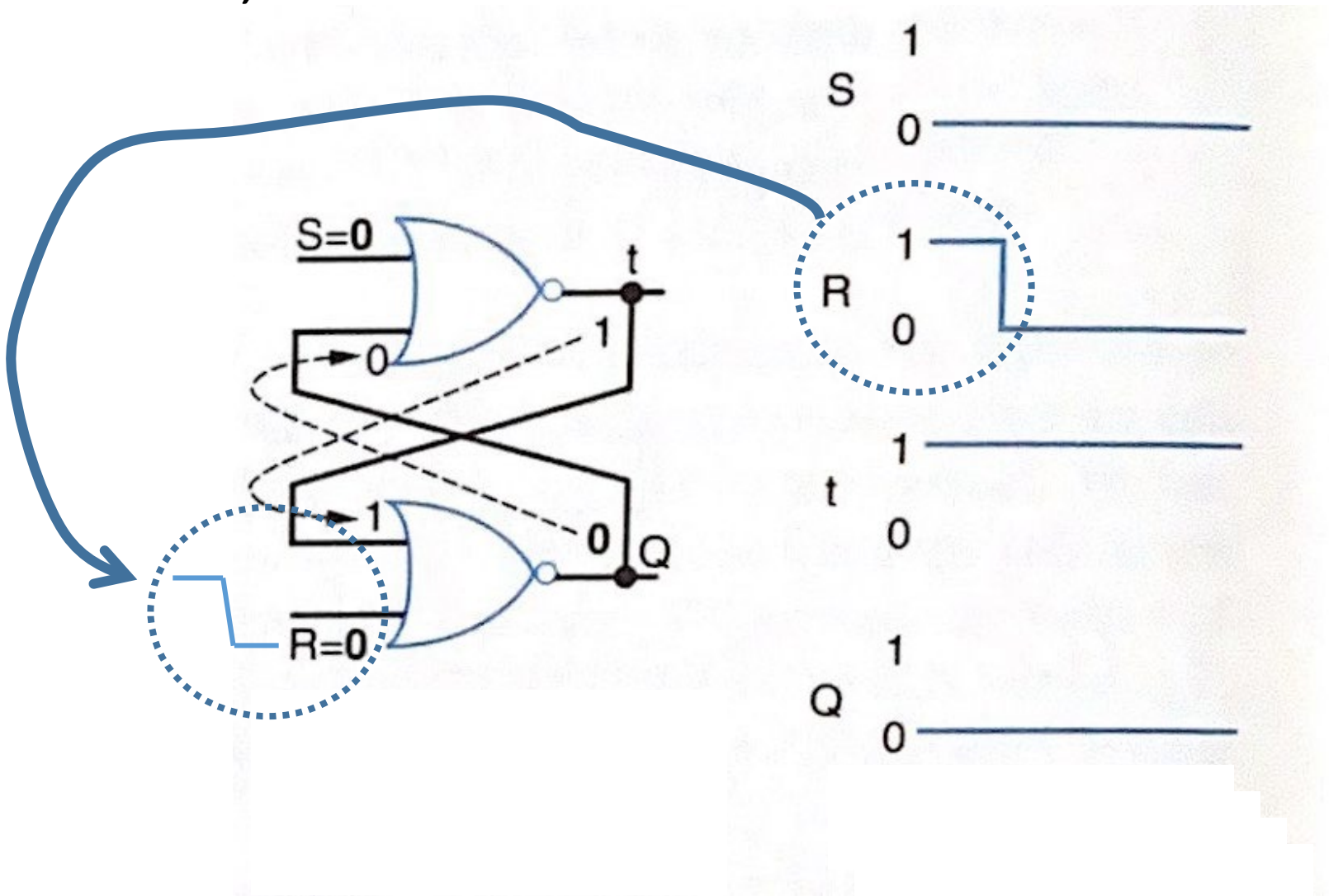




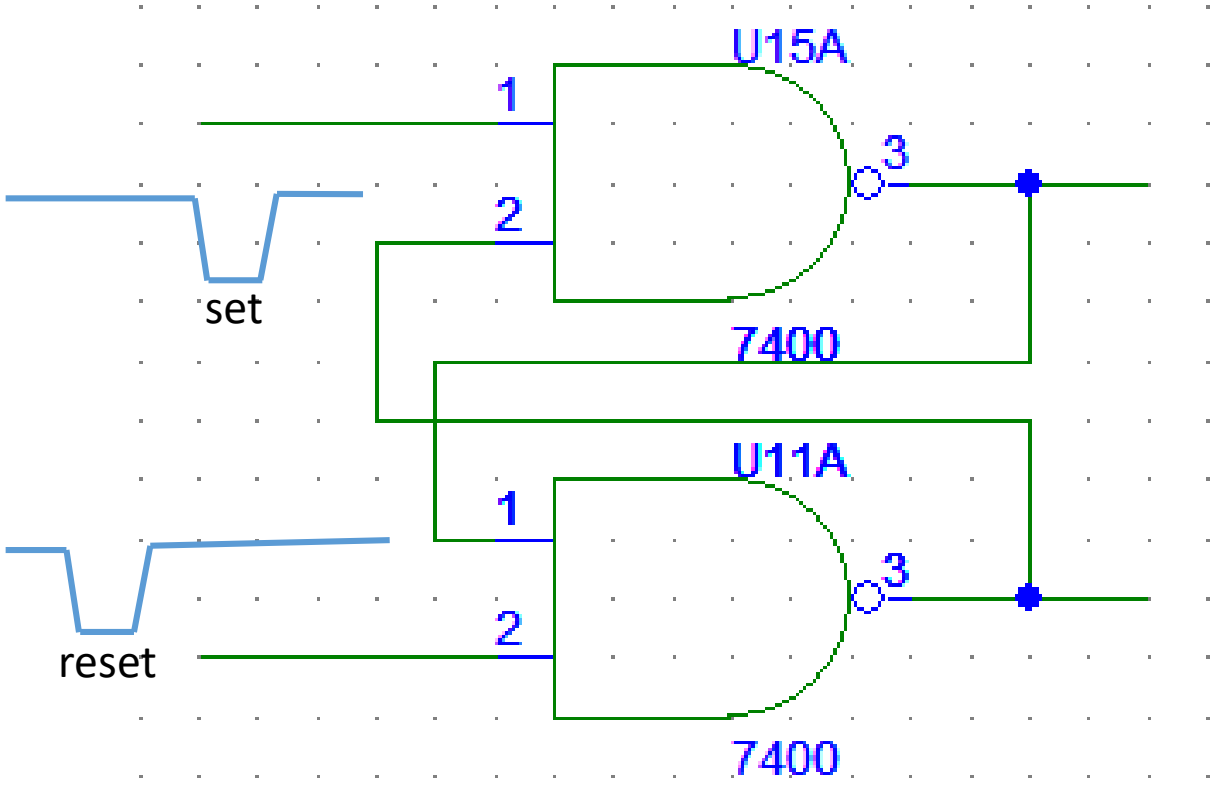


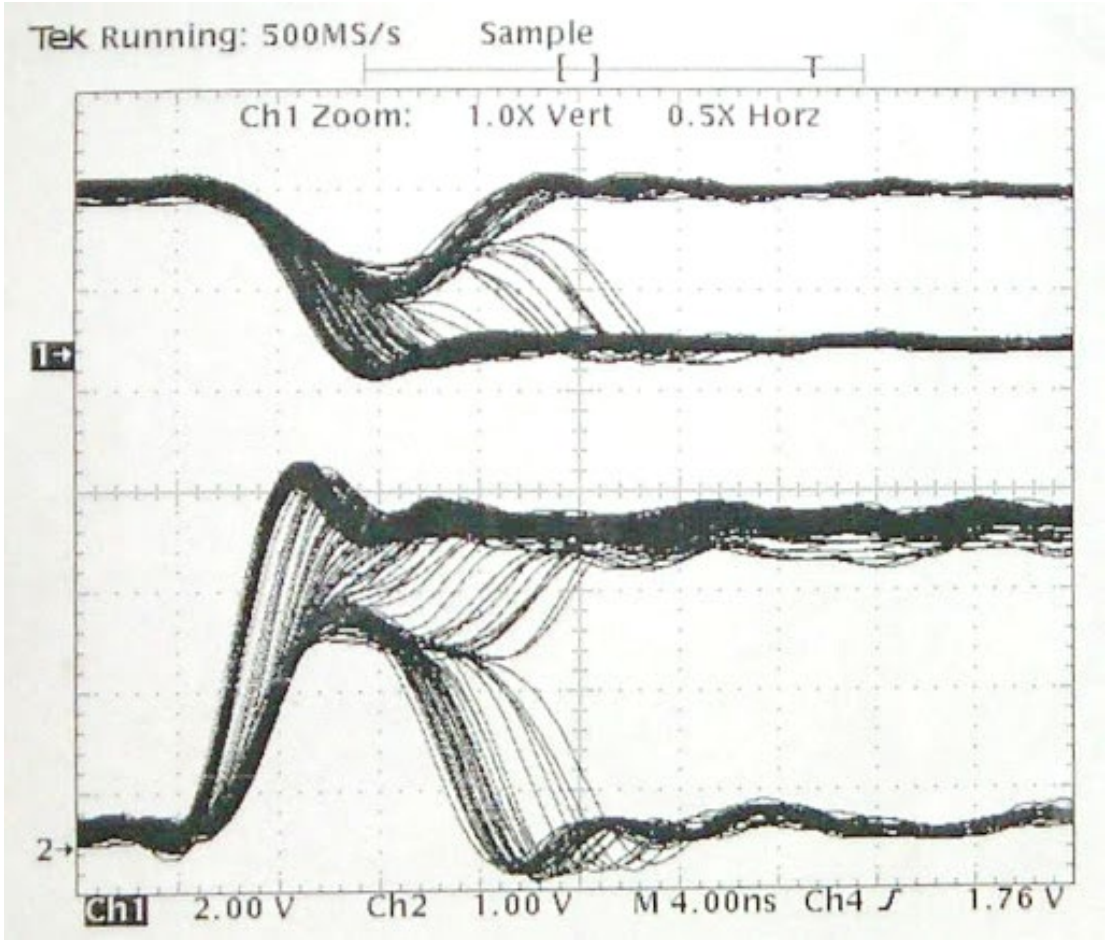


Idle: S=0, R=1->0



Latches S/R: effetto della durata degli impulsi





- La durata degli impulsi di comando è fondamentale per garantire il corretto funzionamento del latch

Metastabilità

Correspondence

Anomalous Behavior of Synchronizer and Arbiter Circuits

THOMAS J. CHANEY AND CHARLES E. MOLNAR

Abstract—**Observations are shown of oscillatory and metastable behavior of flip-flops in response to logically undefined input conditions such as those that occur in synchronizers and arbiters. Significant systems failures have resulted from this fundamentally inescapable problem that is generally not appreciated by system designers and users.**

Index Terms—**Asynchronous interactions, binary switching time, flip-flop metastable region, interrupt failure, synchronizer failure mode.**

Discussion at a recent Workshop on Synchronizer Failures (Washington University, St. Louis, Mo.; April 27–28, 1972) has revealed that a number of computer systems made by several manufacturers are subject to significant rates of system failure that result from unreliable interactions between mutually asynchronous subsystems. Multiproces-

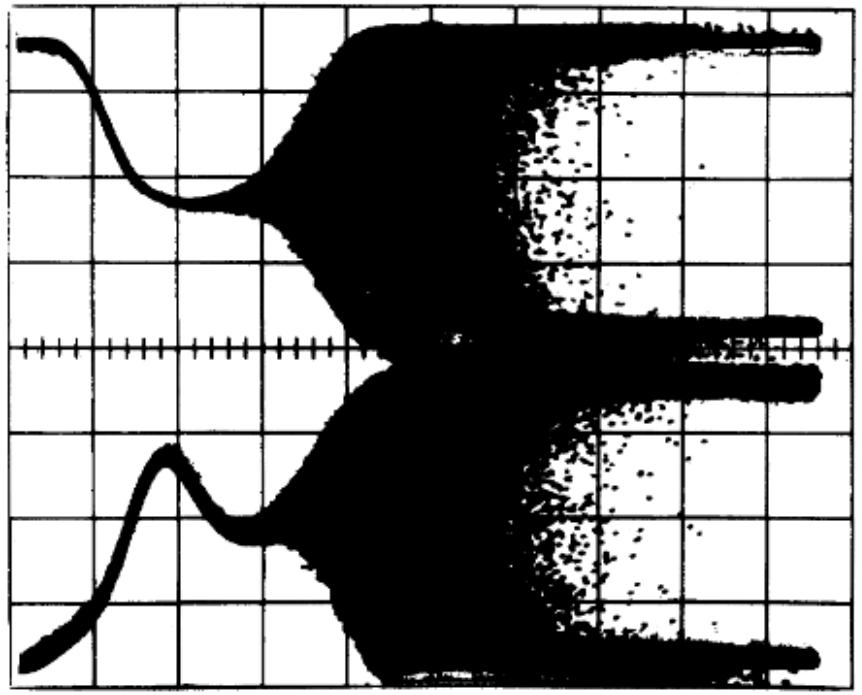
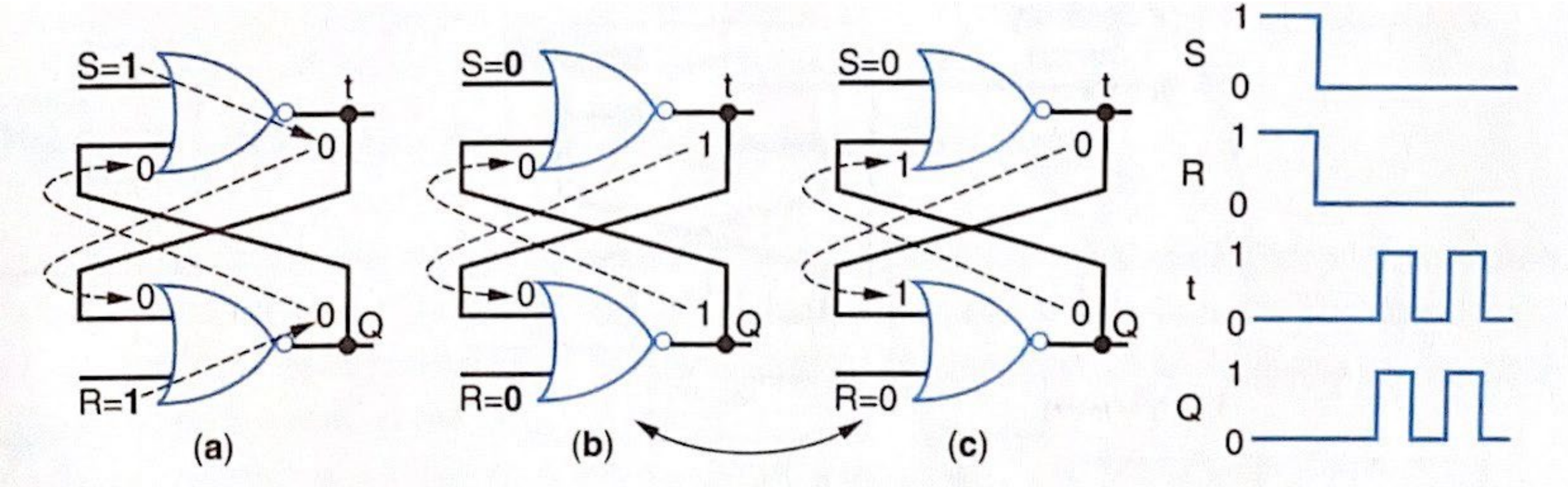


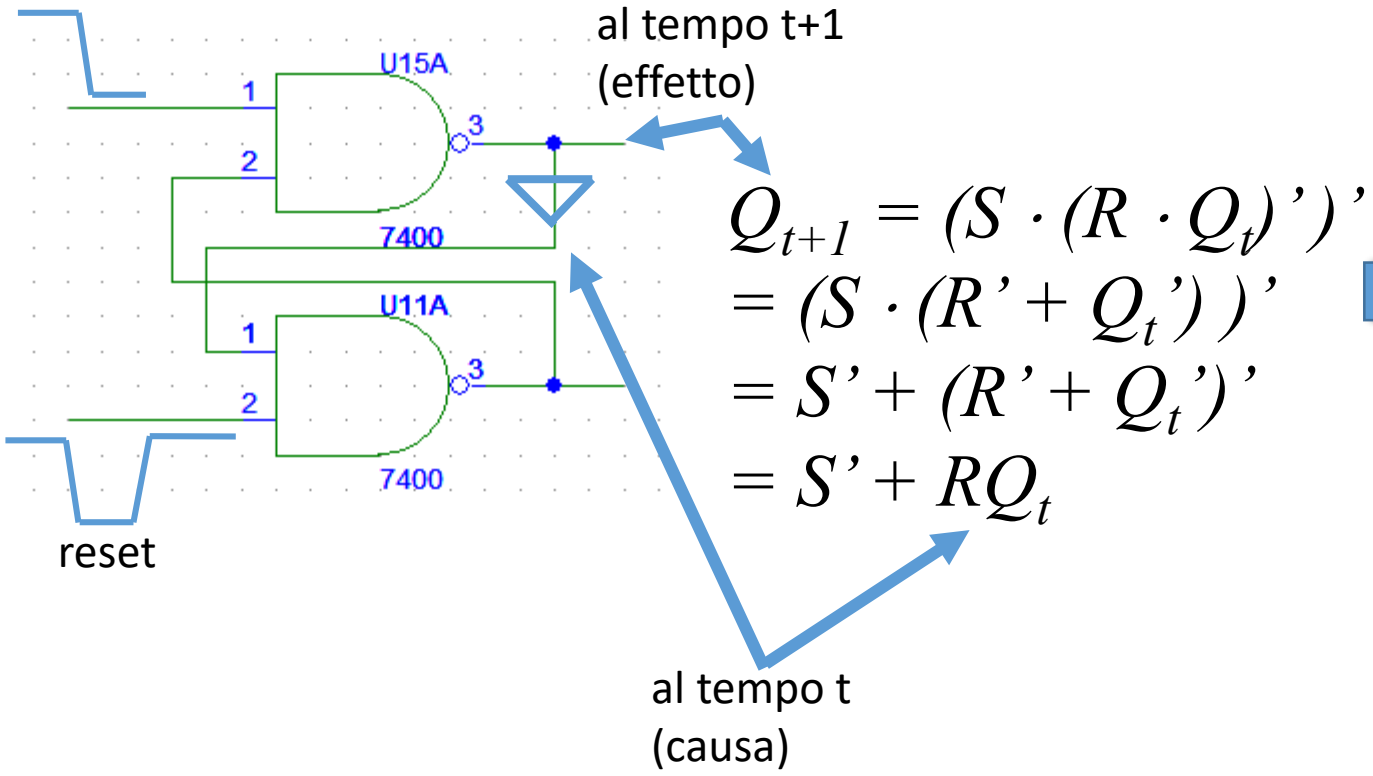
Fig. 1. Q and $\overline{Q}$ of ECL clocked R-S flip-flop with clock and data inputs changing simultaneously (5 ns/div, 0.25 V/div).

Latches S/R (NOR): (1,1) → (0,0)

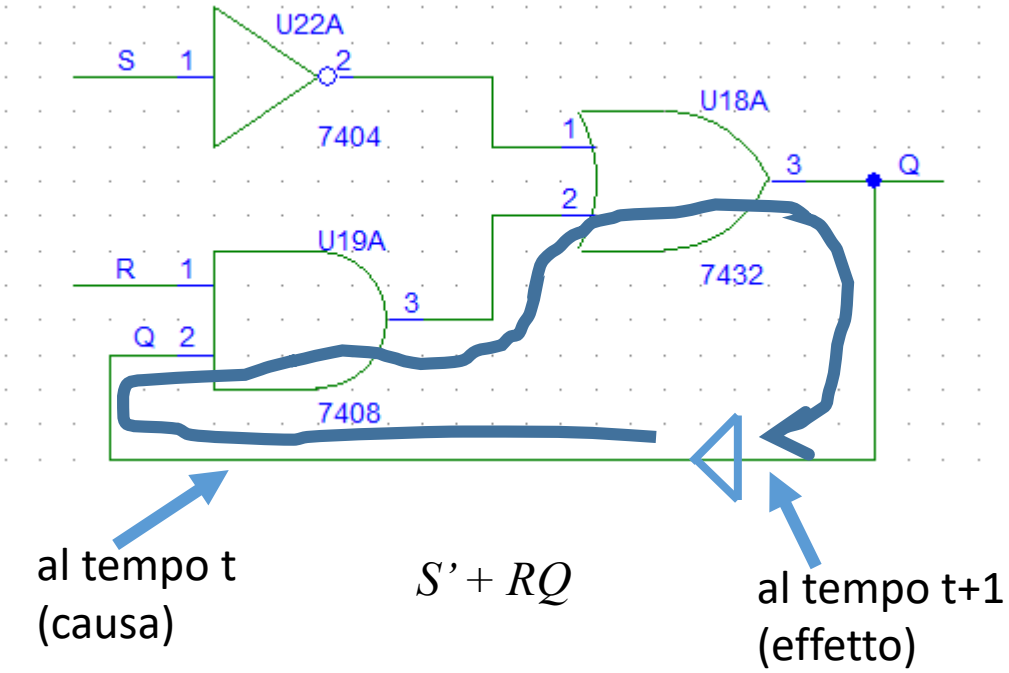


- Una commutazione simultanea (ideale, irrealizzabile in pratica) di set e reset può generare una condizione metastabile
- Il latch può oscillare per un periodo di tempo che dipende della tecnologia costruttiva

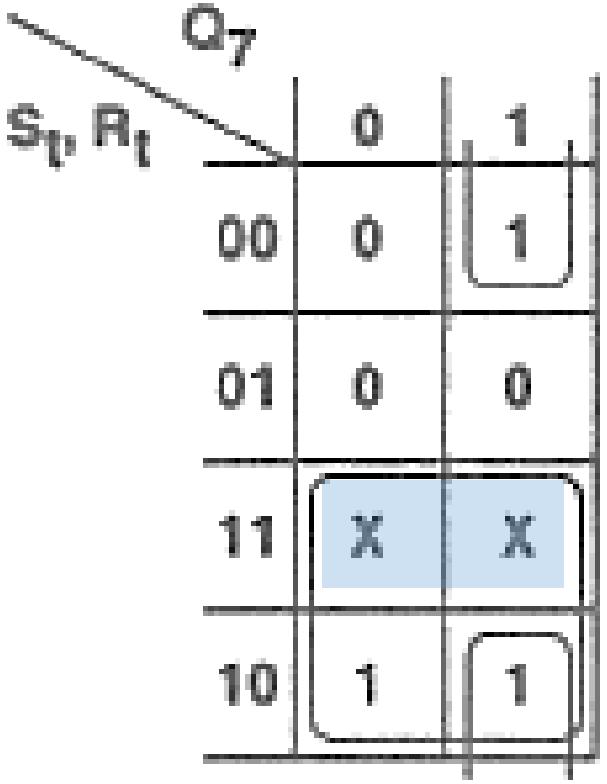
Forma SoP



$$Q_{t+1} = (S \cdot (R \cdot Q_t)')'$$
$$= (S \cdot (R' + Q_t'))'$$
$$= S' + (R' + Q_t')'$$
$$= S' + RQ_t$$



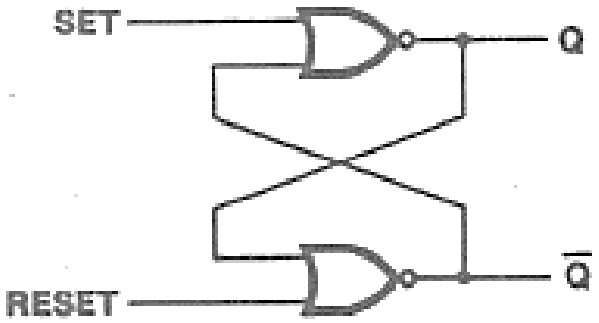
Transition Table



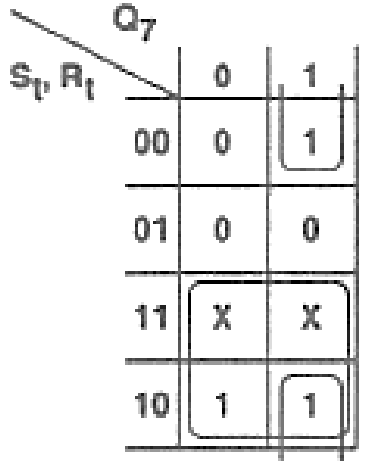
$Q_{t+1} = S_t + Q_t^* / R_t$

(where, $S_t^* R_t = 0$)

(c)



(a)



$Q_{t+1} = S_t + Q_t^* / R_t$

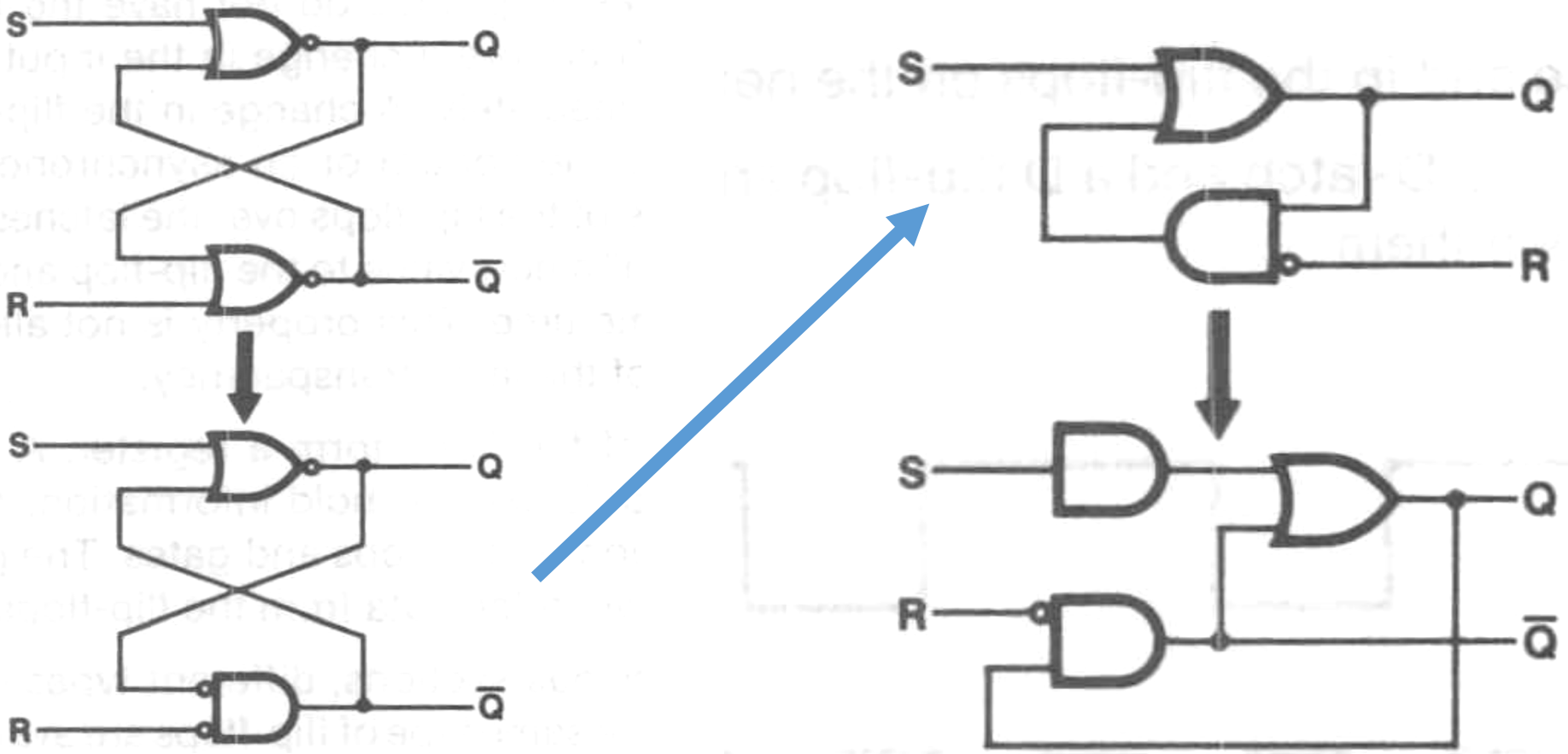
(where, $S_t^* R_t = 0$)

(c)

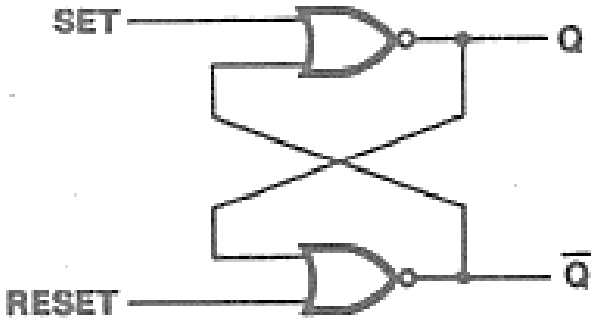
St	Rt	Q_t	Q_{t+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

(b)

SoP form



NOR → NAND

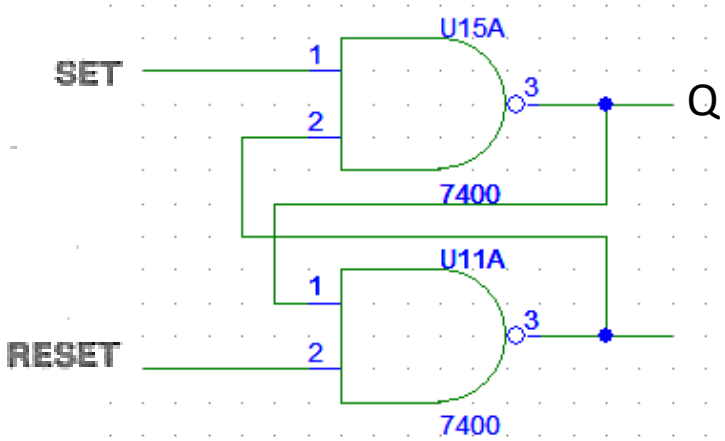


S_t, R_t \ Q_7	0	1
00	0	1
01	0	0
11	X	X
10	1	1

$$Q_{t+1} = S_t + Q_t^* / R_t$$

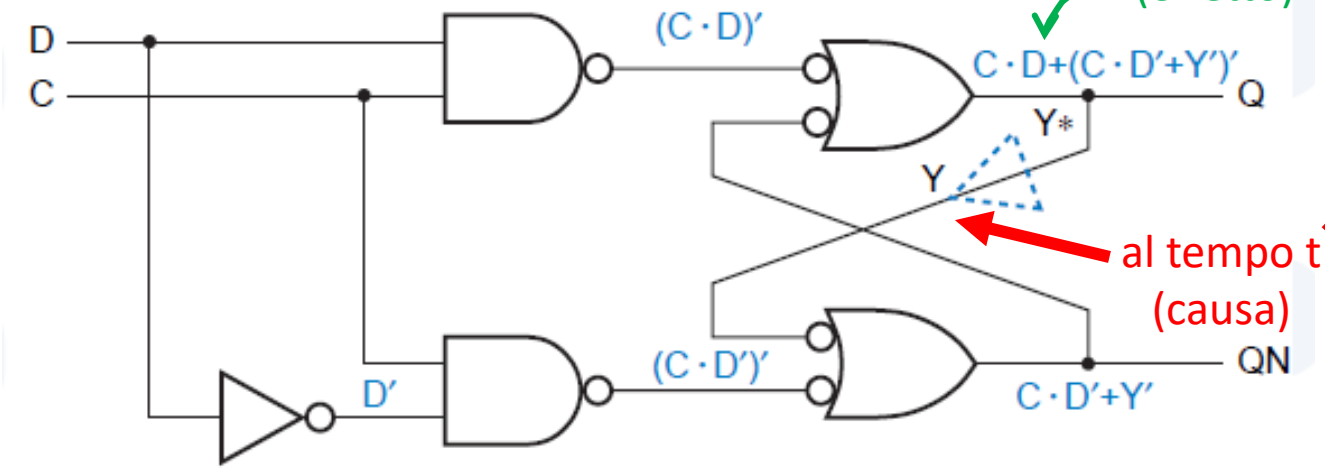
(where, $S_t \cdot R_t = 0$)

(c)



SR	Qt=0	Qt=1
00	X	X
01	1	1
11	0	1
10	0	0

D Latch *with enable*

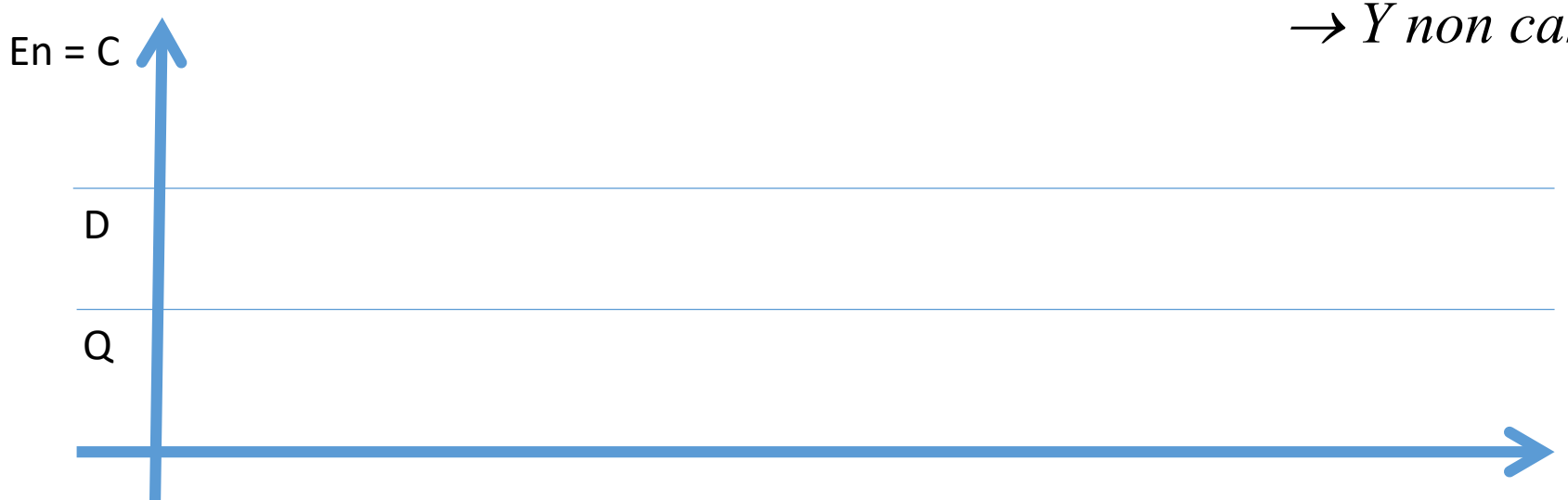


Transition table

	C D			
Y	00	01	11	10
0	0	0	1	0
1	1	1	1	0
	Y*			

enable = 0
→ Y non cambia

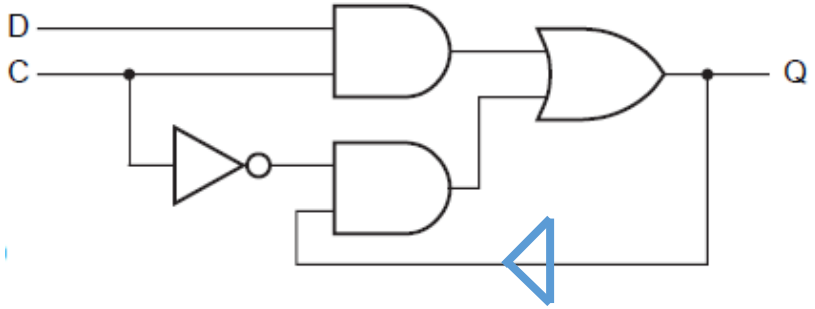
enable = 1
→ Y = D
(trasparenza)



D-Latch in forma SoP

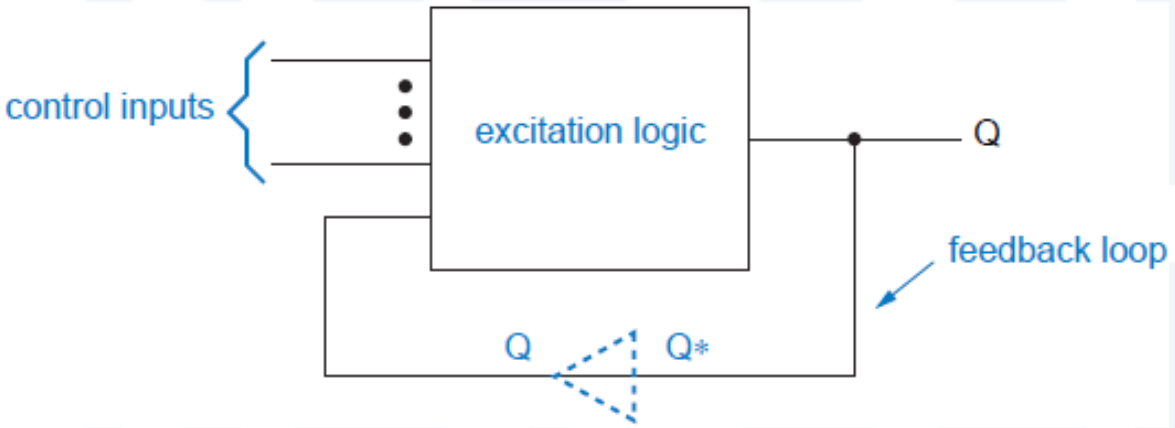
	C D			
Y	00	01	11	10
0	0	0	1	0
1	1	1	1	0
			Y*	

D Latch with enable



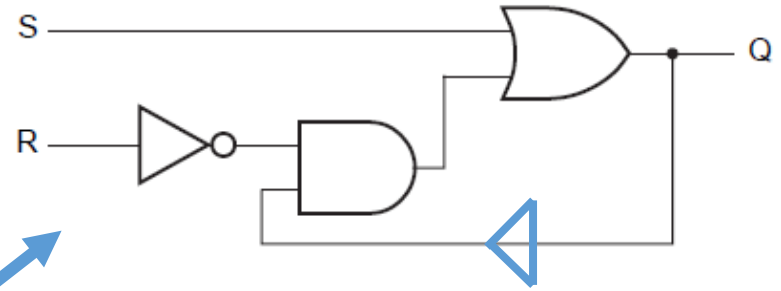
$$Q* = C \cdot D + C' \cdot Q$$

Latch architecture



$$Q^* = (\text{forcing term}) + (\text{holding term}) \cdot Q$$

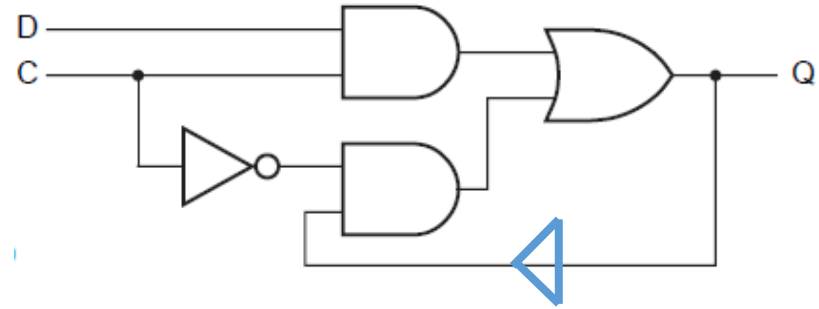
SR Latch



$$Q^* = S + R' \cdot Q$$

$$Q^* = C \cdot D + C' \cdot Q$$

D Latch with enable



D-Latch timing arcs

SN5475, SN5477, SN54LS75, SN54LS77
SN7475, SN74LS75
4-BIT BISTABLE LATCHES
SDLS120 – MARCH 1974 – REVISED MARCH 1988

FUNCTION TABLE
(each latch)

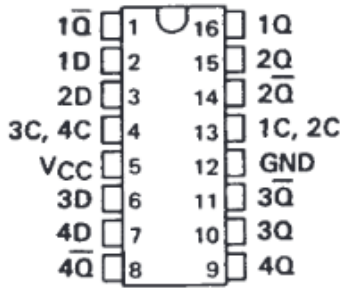
INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

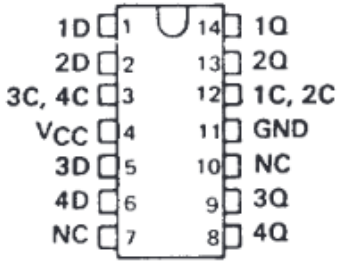
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

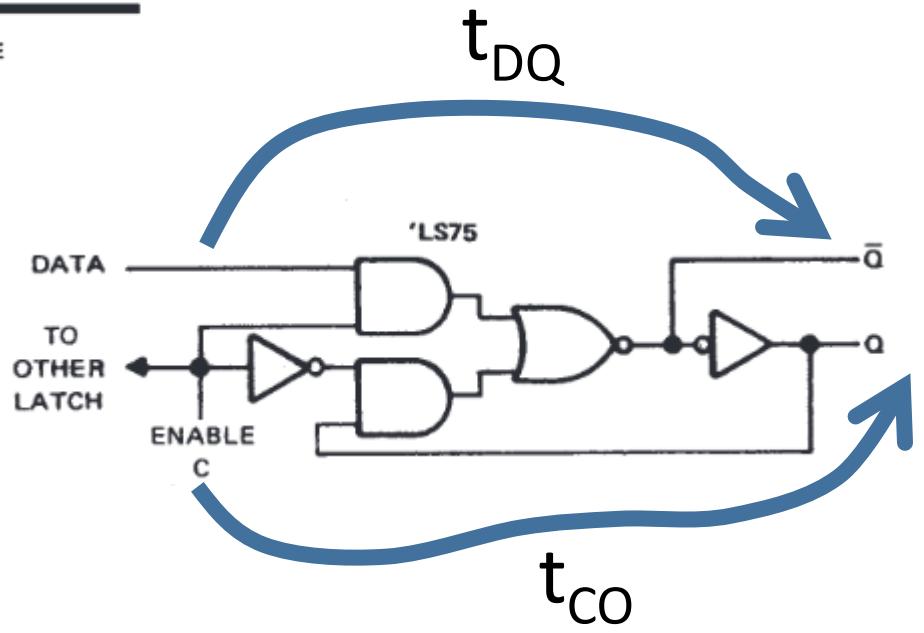
SN5475, SN54LS75 . . . J OR W PACKAGE
SN7475 . . . N PACKAGE
SN74LS75 . . . D OR N PACKAGE
(TOP VIEW)



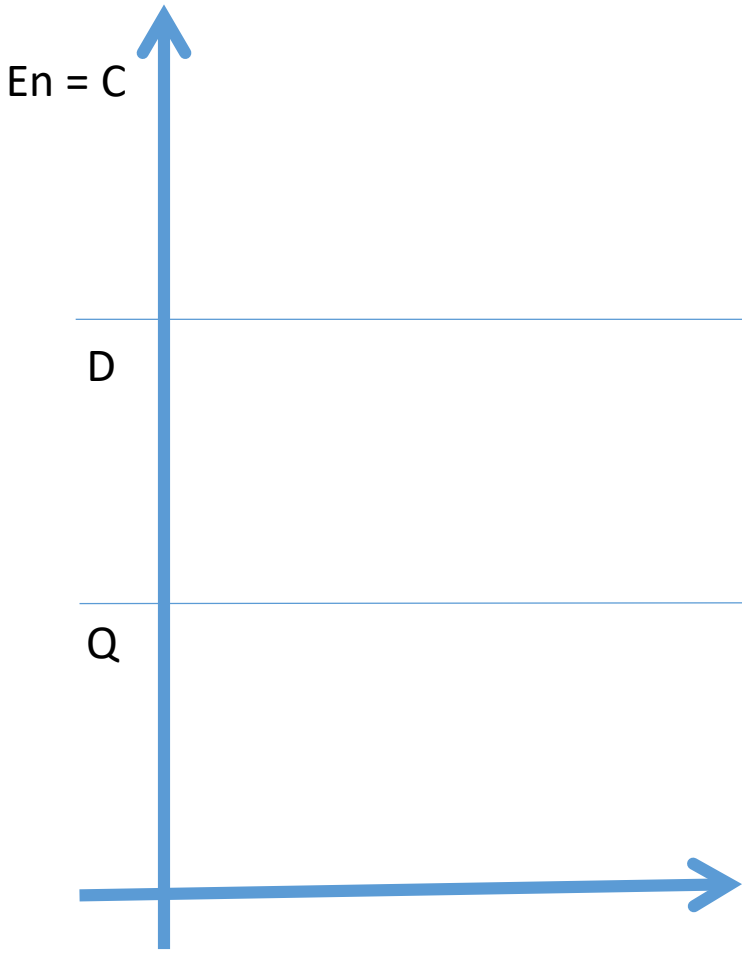
SN5477, SN54LS77 . . . W PACKAGE
(TOP VIEW)



NC - No internal connection

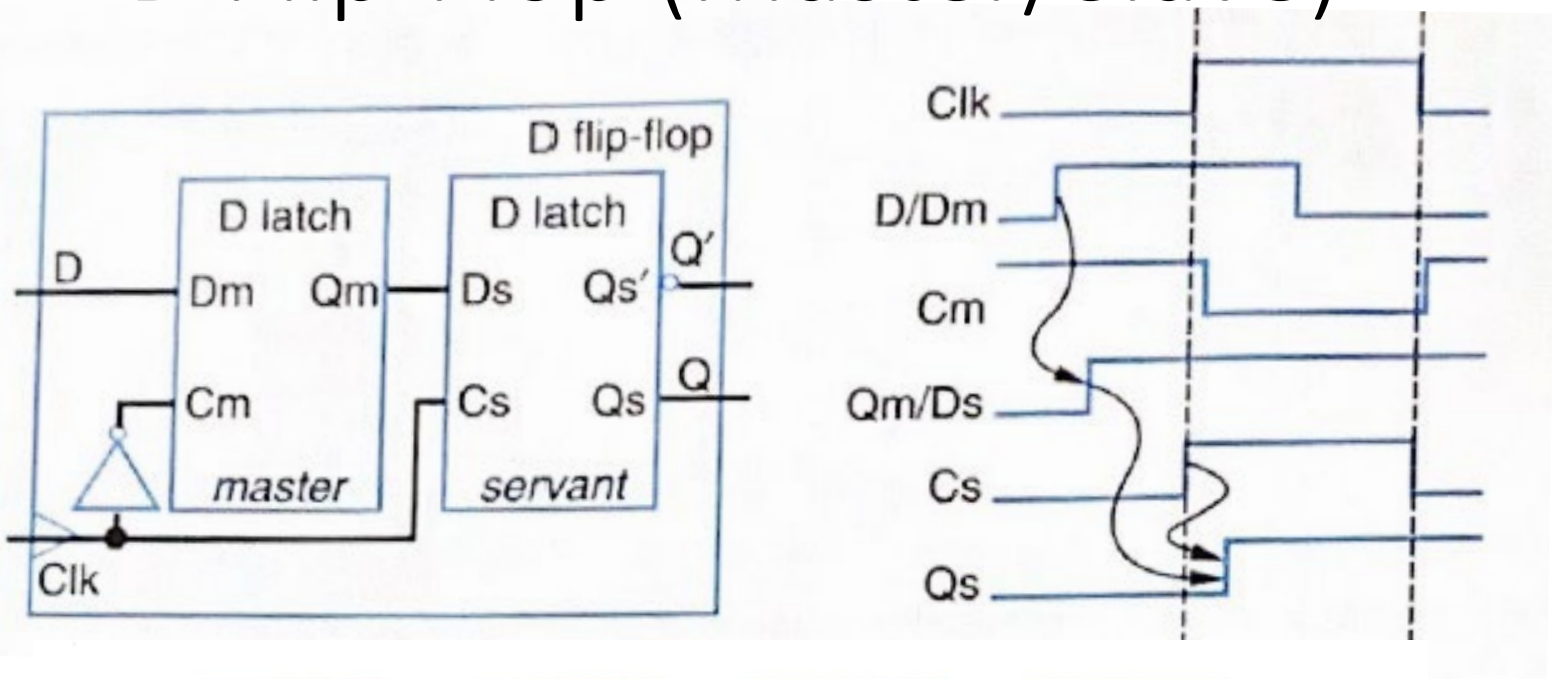


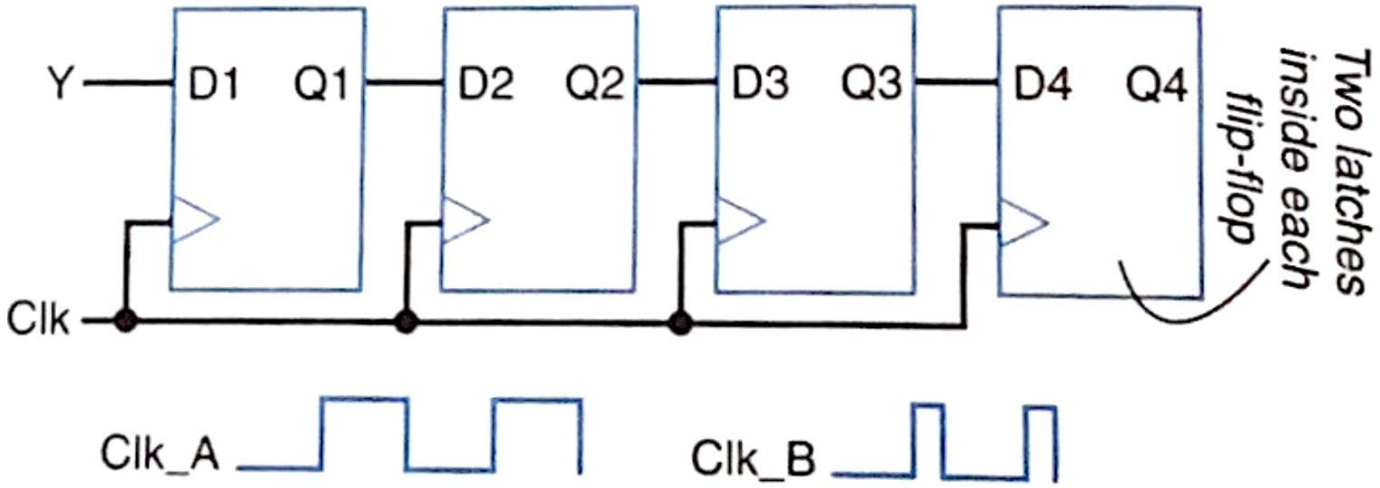
D-Latch Timing /2



	From:	To:	TTL 'LS75	TTL 'ALS373	ECL F100130	CMOS MM54/74	CMOS HC75
						Typ.	Max.
Setup time, t_{su}			20	10	0.70	12	20
Hold time, t_h			5	7	0.60	−2	0
Control pulse width, t_w			20	10	2.00	10	16
			Typ. Max.	Typ.	Min. Max.		
t_{PLH}	D	Q	15 27	8	0.50 1.70	10	25
	D	$\overline{Q}$	12 20		0.50 1.70	12	22
	C	Q	15 27	13	0.75 2.00	18	29
	C	$\overline{Q}$	16 30	13	0.75 2.00	13	25
t_{PHL}	D	Q	9 17	Same	Same	14	23
	D	$\overline{Q}$	7 15	as	as	10	20
	C	Q	14 25	t_{PLH}	t_{PLH}	16	27
	C	$\overline{Q}$	7 15			11	23

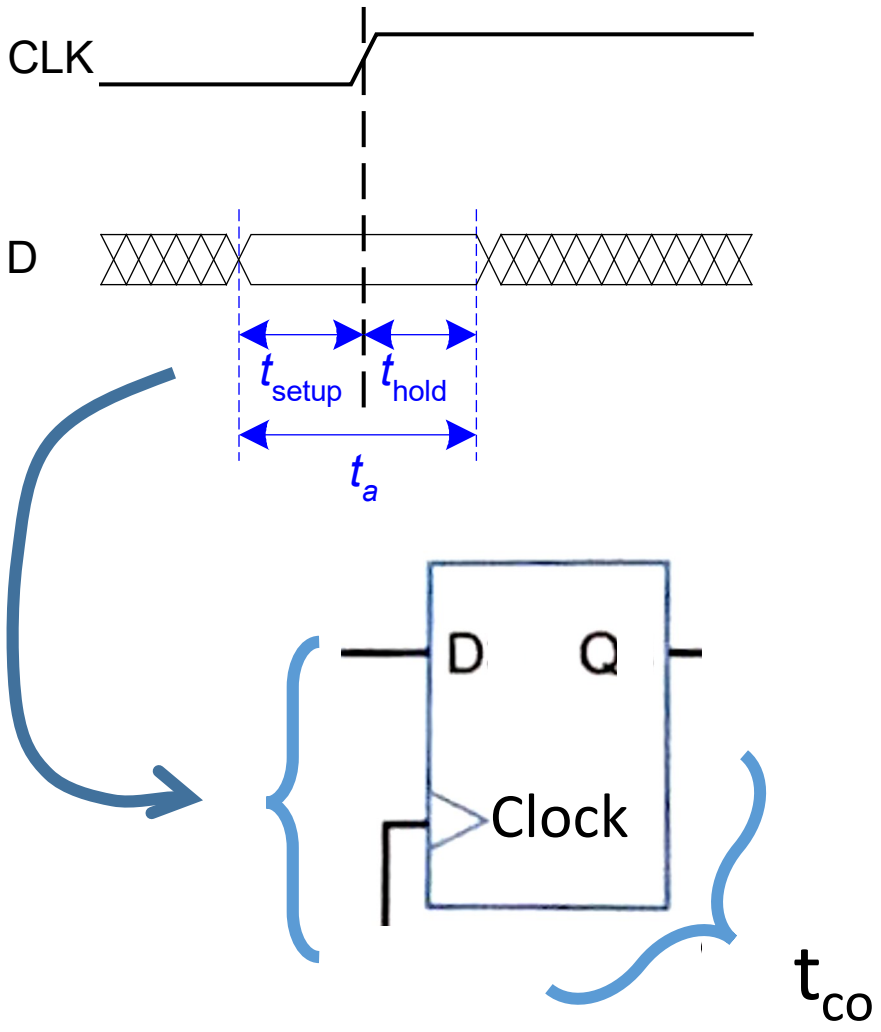
D Flip-Flop (Master/Slave)





- L'architettura Master/Slave è una delle possibile realizzazioni che esibisce un comportamento edge-triggered
- Il Flip-flop eredita le principali caratteristiche timing dei D-latch di cui è costituito:
  - t_{setup}
  - t_{hold}
  - t_{width}

D Flip-flop timing



- **Setup time:** t_{setup} = il dato deve essere stabile *prima* del fronte attivo del clock
- **Hold time:** t_{hold} = il dato deve essere stabile *dopo* il fronte attivo del clock
- **Aperture time:** t_a = tempo complessivo nel quale il dato deve essere stabile ($t_a = t_{setup} + t_{hold}$)
- **Clock-to-output:** t_{CO} = ritardo tra il fronte attivo del clock e la presentazione del nuovo dato su Q

D-FF timing /1

SN7474, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

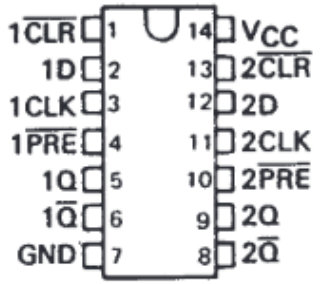
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

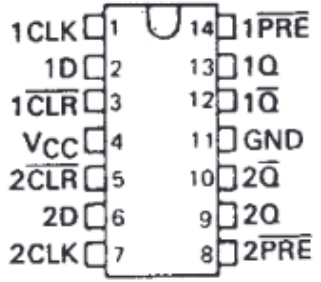
These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)



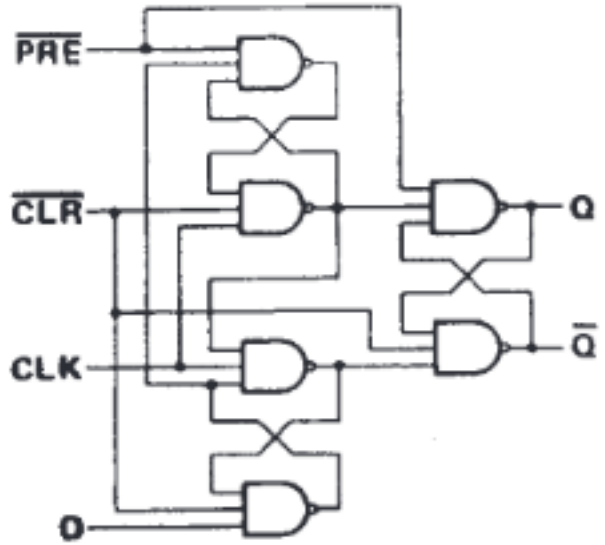
SN54LS74A, SN54S74 . . . FK PACKAGE

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

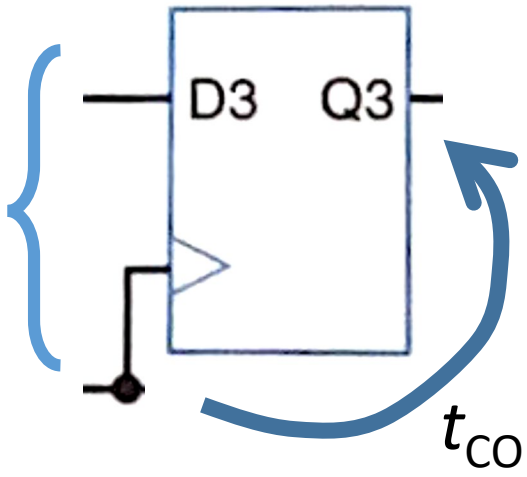
† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic diagram (positive logic)



D-FF timing /2

t_{setup}
t_{hold}



SN5474, SN54LS74A, SN54S74
SN7474. SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR
SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

			SN5474			SN7474			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	30			30			ns
		CLK low	37			37			
		$\overline{PRE}$ or $\overline{CLR}$ low	30			30			
t_{su}	Input setup time before CLK ↑		20			20			ns
t_h	Input hold time-data after CLK ↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

switching charateristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	25		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$				25	ns
t_{PHL}						40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			14	25	ns
t_{PHL}					20	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.