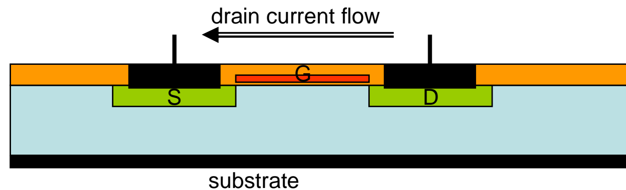
The Power MOS

What are the main differences between a MOS device for signal application and a power MOS?
In a signal MOS, as indicated in figure, the device is realized on the top surface of the chip, with both Source and Drain contacts on top, and the current flow is transverse to the chip surface (and not perpendicular to it); the bottom contact (substrate) is not collecting any current.



As a result we have two drawbacks in using this structure for high current and voltages:

a) the current is not flowing in the chip area, but only in the very thin channel under the gate, and we can increase the current only by increasing the lateral channel width W, not the chip area.
b) the Drain voltage is limited by the channel length L, that must be no more than some microns to have a significant current in ON state (remember that the MOS current factor K is proportional to W/L): as a result the max drain voltage is limited by breakdown of the Drain junction to less than tens of volts.

For power (and higher voltages) applications, the basic MOS structure must be largely modified, leading to a vertical device (VDMOS) as for the other power devices seen before.

Let's recall briefly the main relationships for the IV characteristics of a signal MOS

The threshold voltage V_T:

$$V_T = \Phi_{GS} + \phi * - \left(\frac{Q_{SI}}{C_{OX}} + \frac{Q_{OX}}{C_{OX}} \right) \qquad (1)$$

is an increasing function of the oxide thickness (through C_{OX}) and of the body doping (through Q_{SI}.
For V_{GS}>V_T the channel is formed and the Drain current I_D can flow. Its dependence on the Drain voltage V_{DS} up to the pinch-off is:

$$I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] = K \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] \qquad (2)$$

Above the pinch-off $(V_{DS} \geq V_{GS} - V_T)$ the current I_D remains constant at the limit value:

$$I_D = K \left[V_{GS} - V_T \right]^2 \qquad (3)$$

(neglecting the channel modulation after the pinch-off)

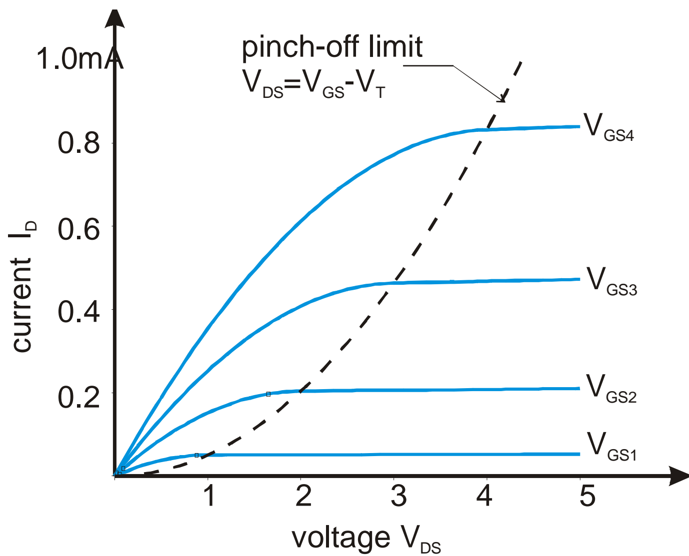


Fig. 1

From eq. (2) and (3) a typical set of IV curves for a signal MOS is plotted in figure, assuming V_T = 1V, $K_n = 50\cdot 10^{-5} A/V^2$, and a channel ratio W/L = 1.
To increase the output current I_D in the range of tens of amps, we need to have an equivalent channel width W 10^4 times the channel length L (in the range of few microns), about tens of millimeters.
This is usually accomplished by putting 10^4 elementary MOS in parallel; as a result the MOS for high currents is made of many elementary cells (as for the BJT).

The initial slope of the output IV curves is linear (see eq. (2)) and we can define a R_{ON} resistance for each curve from the linear slope as:

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{2K(V_{GS} - V_T)} = \frac{L}{\mu_n C_{OX} W (V_{GS} - V_T)} \qquad (4)$$

The structure of Power MOS

The Power MOS differs basically from the signal MOS because it has to withstand higher voltages: then the drain is moved to the bottom part of the chip, and a low doped (epitaxial) region N^- is added to sustain the drain voltage V_{DS} .
A typical structure of a basic cell for a Vertical Diffused Power MOS (VDMOS) is reported in the figure (actually two elementary MOS are inserted in the cell, acting in parallel). For each MOS:

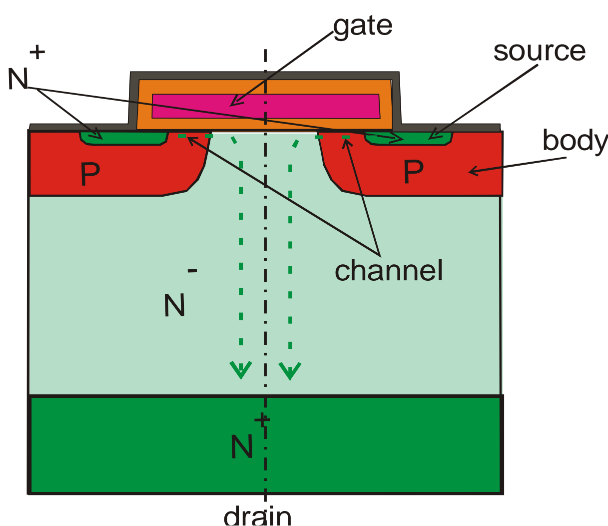


Fig. 2

a) the body is not the chip substrate, but it is made by a P type diffusion into the epi layer, in a window of limited lateral space to allow an N layer to be present on top.
b) The drain contact is realized on the bottom of the chip, on a N^+ layer that is the actual chip substrate
c) an N^- epitaxial layer has been made on top of the N^+ substrate with doping and thickness to allow a substantial drain voltage, as we will see.
d) the channel is induced at the top surface in the P body by effect of the V_G applied to the gate. The electrons flowing into the channel travel through the epi layer and are then are then collected by the drain

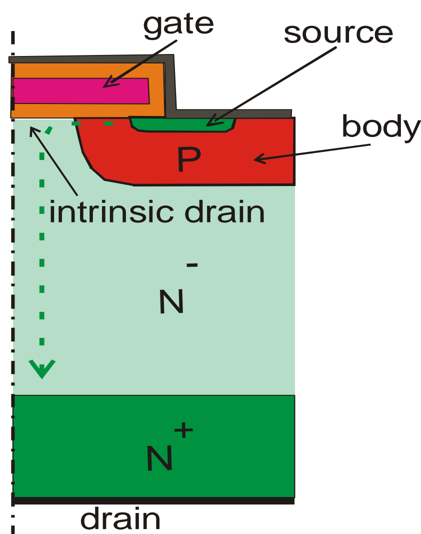


Fig. 3

With reference to the half cell structure, we can consider the N^- region on top surface as an "intrinsic Drain" that collects the electrons flowing through the channel induced by the gate. Then the electrons (majority carriers) will travel into the epi layer to the N^+ layer that acts as the Drain electrode.
The Body is made by P implant and diffusion in the N^- epilayer; the surface doping will affect the threshold voltage V_T.
The Source is made by a second N^+ diffusion into the body region, and the top metallization will make a contact between the source and the body so there will be no body effect on the threshold voltage for the discrete Power MOS device.
The polysilicon Gate, over the thin oxide layer, will be extended not only above the channel of the body region, but also on the intrinsic drain region between the two following cells: this will make some negative and positive features as we will see later.
The Drain contact is made on the bottom surface of the chip, by a metallization on the N^+ layer (actually the wafer substrate of a thickness of some hundred microns), to make an ohmic contact (and not a schottky barrier).

The Power MOS device is then made of many elemental cells (each containing 2 lateral MOS channels), closely packed to cover the whole chip area, and all connected in parallel by the common Drain and source metallization, as reported in the figure, where:

A: elementary cell pitch
W: cell width
L: channel length
N: number of elementary cells
Total chip area: N·A·W

The total drain current in pinch-off is 2N times the current of each lateral MOS : $k_n \frac{W}{L}(V_{Di} - V_T)^2$ where V_{Di} is the intrinsic drain voltage.

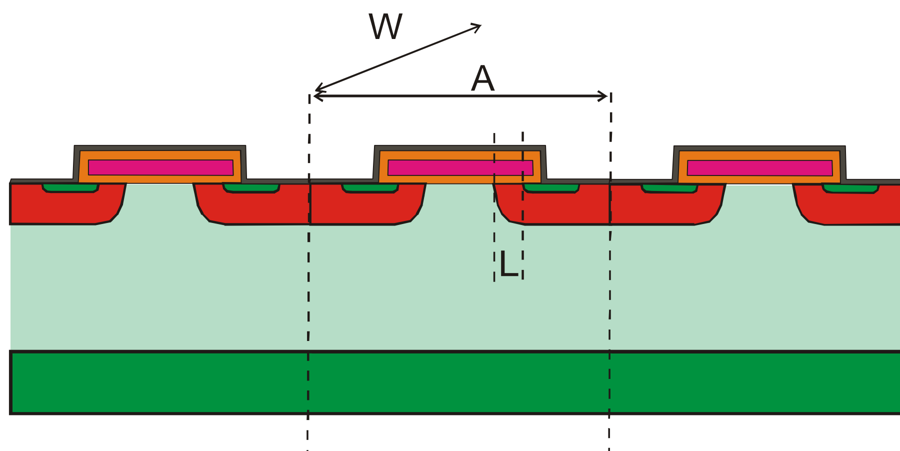


Fig. 4

OFF state max Drain voltage

The max Drain voltage in the OFF state ($V_{GS}<V_T$) is the max reverse voltage that can be sustained by the body/epi P/N junction, that is reverse biased (the source/body junction $V_{SB}=0$). The epi layer must then have a doping and thickness such as to sustain the V_{DSMAX} required.
To avoid the negative effects on V_{BR} due to the body curvature (as for the PIN junction termination) that could arise as sketched in fig. 5b, the poly gate is extended over the intrinsic Drain area N^- (fig. 5a). In this way the gate acts as a field plate (with a thin oxide layer t_{OX}) and creates a depletion layer underneath this area, that will strongly reduce the curvature of the equipotential line, and gives a breakdown value very near to the plane case.

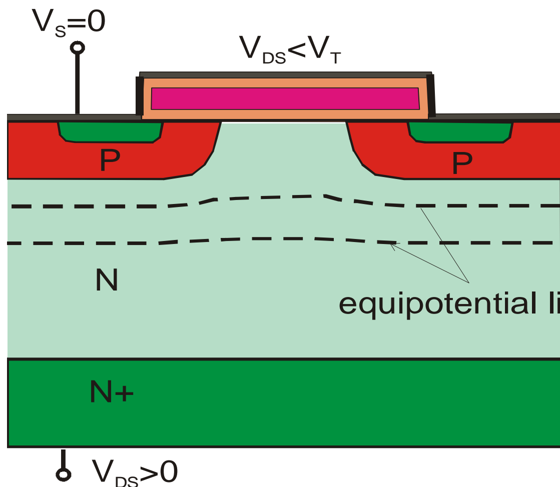


Fig. 5a: with extended gate structure

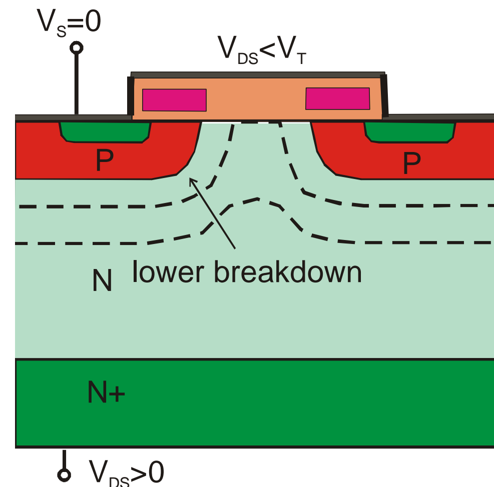


Fig. 5b: with gate only on the channel

Assuming a negligible curvature of the equipotential lines due to the extended gate structure, as in fig. (a), the max drain voltage (at the bottom drain electrode) is limited by the breakdown value of the PN^-N^+ vertical structure between body and drain.
This structure corresponds to a PIN diode, and in fact it is a PIN diode integrated into the MOS structure; his breakdown value then is dependent on the doping N^- and thickness W_D of the epi layer, the same way as seen for the PIN diode.

It must be pointed however that this added layer contributes to a significant voltage drop when the MOS is in conducting state, because for the MOS we can not rely on the conductivity modulation to reduce the ohmic drop, so one must be careful in selecting the best doping and thickness values that gives the desired V_{DSMAX} (the PIN diode breakdown voltage) in the OFF state, while keeping as low as possible the voltage drop in ON state (i.e. when the MOS is conducting, and a drain current is flowing into this layer).

The presence of the low doped epi layer is one of the main points that make the power MOS different from the signal MOS, and its effect is more relevant on devices that must sustain high voltages, than on devices designed for low voltage, high current, as we will see.

ON state conduction losses of the VDMOS

The voltage drop presented in ON state causes a power dissipation that is the main limiting factor for low frequency operation. So it is important to know the different components that give the overall ON state resistance R_{ON} of the power MOS and their dependence on the device structure, as well as on the max voltage.

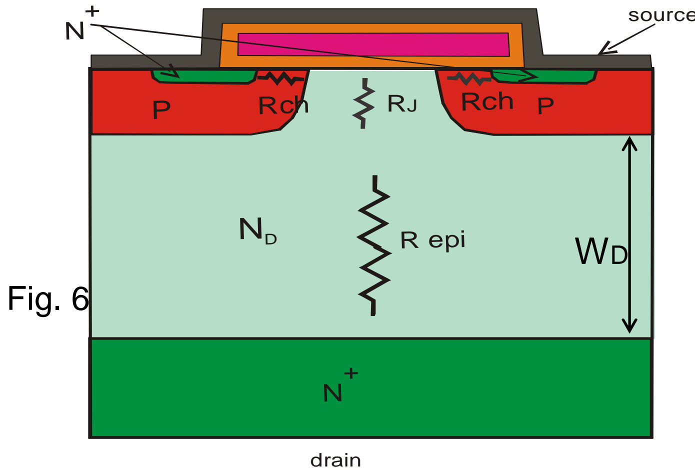


Fig. 6

With reference to the general VDMOS cell structure indicated in figure, we can define 3 main components of the resistance R_{ON} presented in conducting state at low drain voltage ($V_{GS}>V_T$, $V_{DS} <V_{GS}$) :

a) the channel resistance due to the electron flow into the channel (already seen in signal MOS), indicated as R_{ch}.
b) b) the JFET region resistance due to the electron flow into the N^- region that separates the two following P body regions, indicated as R_{JFET}
c) the epi resistance due to the electron flow into the epi layer of thickness W_D down to the Drain, indicated as R_{epi}

$$R_{ON} = R_{ch}+R_{JFET} + R_{epi}$$

R_{ON} components:

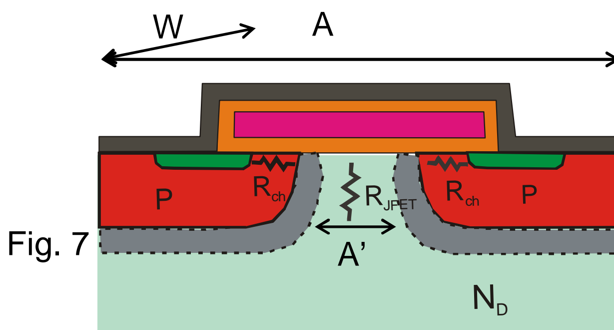


Fig. 7

It is useful to normalize the resistance values to the chip area, by defining a specific resistance multiplied by the elementary cell area R_{sp} = R·A·W, expressed in ohm·cm².
With reference to fig. 7 where the first two component are indicated, we have:

R_{chsp} = the resistance offered by the channel is the one presented by the signal MOS in the linear part of the I_DV_{DS} curve, and is defined by eq (4). The expression of the R_{chsp} is then:

$$R_{CH}sp = \frac{L \cdot W \cdot A/2}{\mu_n C_{OX} W (V_{GS} - V_T)} = \frac{L \cdot A}{2\mu_n C_{OX} (V_{GS} - V_T)} \quad (5)$$

and it can be decreased if the cell area A is reduced (increasing the cell density per chip)

R_{JFETsp} = the resistance of the vertical region between the two P region, named after the JFET effect in that region: the depletion regions across the PN junction make smaller the width A' of the vertical channel and increase the resistance of this channel.
The relative value of this component will increase if the area cell A is reduced, because the vertical channel width A' is reduced and the lateral depletion will have a stronger effect.

R_{episp} = the resistance ef the epi layer, as indicated in fig. 6. Assuming for the vertical electron flow an uniform distribution across the whole cell area (a strong approximation, because the initial flow is coming by the reduced width A' of the JFET region, respect to the whole cell width A), R_{episp} is the resistance for unit area of the epi layer of doping N_D :

$$R_{EPIsp} = \frac{W_D}{q\mu_n N_D} \quad (6)$$

The R_{ch} and R_{JFET} components are mainly depending from the pitch A of the elementary cell. The last component depends from the doping N_D and thickness W_D of the epi layer, that are in turn defined by the max voltage V_{DSMAX} requirements for the device.
As a consequence, the R_{EPI} component can be comparable with the other resistance components for a low voltage power MOS, while it will largely increase the R_{ON} value for high voltage device, as indicated by the following table:

Table 1

R_{ON} component	$V_{DSMAX} = 50V$	$V_{DSMAX} = 600V$
R_{ch}	40%	2%
R_{jfet}	30%	1%
R_{epi}	30%	97%

The increase of R_{EPI} (and R_{ON}) with V_{DSMAX} will increase the ON state losses of the Power MOS at high voltage rating, so it is important to define the link between R_{epi} and V_{DSMAX}.

With reference to the breakdown analysis of the PIN diode and to the field distribution of figure 8, the best field profile that gives the best trade-off between a low R_{epi} and an high V_{BR} is the limit case b (NPT case with field going to zero at W_D).

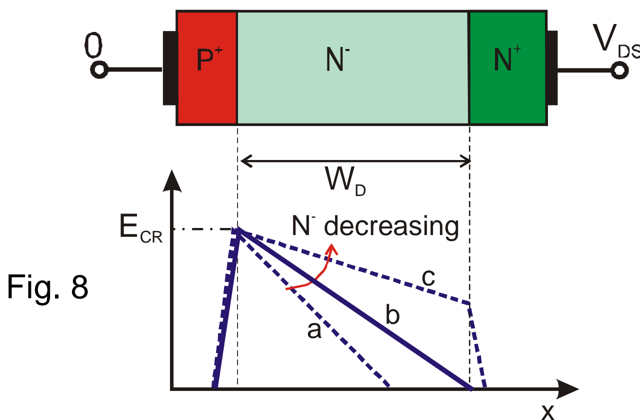


Fig. 8

For this case we have, from the PIN diode analysis:

$$V_{BR} = \frac{E_{CR} W_D}{2}$$

recalling that $E_{CR} = 2{\cdot}10^5$ V/cm, we have for W_D:

$$W_D = 10^{-5} V_{BR} \quad (7)$$

Recalling that N_D is related to V_{BR} for NPT case as:

$$V_{BR} = \frac{1}{2} \frac{E_{CR}^2 \, \varepsilon}{q N_D} \Rightarrow N_D \cong \frac{1.3 \cdot 10^{17}}{V_{BR}} \quad (8)$$

By substituting (7) and (8) in (6) we have the following relationship between R_{episp} and V_{BR}

$$R_{EPI,SP} = \frac{W_D}{q\mu_n N_D} \cong 3 \cdot 10^{-7} (V_{BR})^2 \quad (9)$$

As a result of the previous analysis, we can understand the data of table 1: for the low voltage MOS the epi layer will not affect too much the overall R_{ON} value, and the latter is set by the value of R_{ch} and R_{JFET}; these latter are mainly determined by the cell pitch A and by the cell density of the chip. As an example, for L= 2 µm, A = 30 µm, t_{OX}= 50 nm $R_{,chsp}$ = 0.9 10^{-3} ohm cm^2. The R_{ch} increases slowly with V_{BR} because the channel lenght must be increase for high Voltages to allow the increase in voltage of the intrinsic gain.

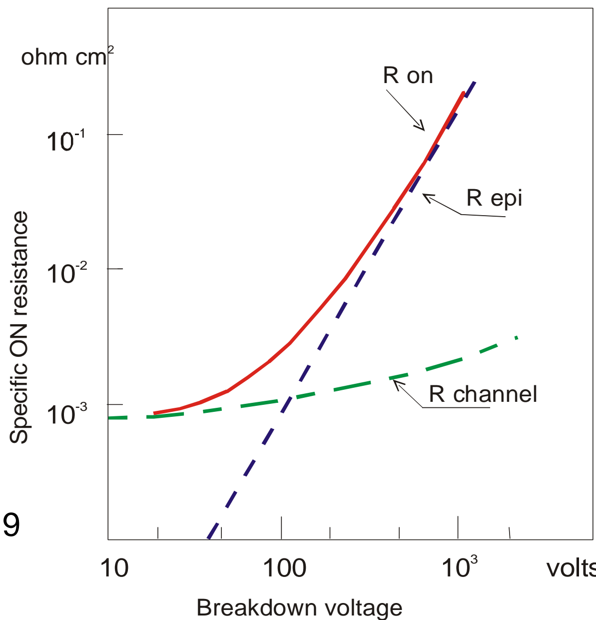


Fig. 9

For voltages higher than 100 V the R_{epi} component becomes relevant and from eq. 8 we find that it will increase with the square law of V_{Br}.

That will lead to unacceptably high values for R_{ON} at voltages above 600V as seen in the plot of fig. 9. As an example, for 600V a R_{ONsp} = 0.1 Ωcm^2 will give a voltage drop of 10 V at a current density of 100 A/cm^2, that is possible for a good Power MOS .

For low voltage applications (V_{DSMAX}< 50 V), the components R_{ch} and R_{JFET} became predominant. To reduce the R_{ON} value for low voltage device, it is customary to increase the cell density on the chip to increase the number of R_{ON} of the elementary cell in parallel (it will increase also the Drain current).

However, the increase of the cell density for a given chip width will need a reduction of the cell pitch A; this decrease will actually reduce the R_{ch} component because the channel length L will be reduced, but will increase the R_{JFET} component because the width A' of he JFET channel is also reduced.

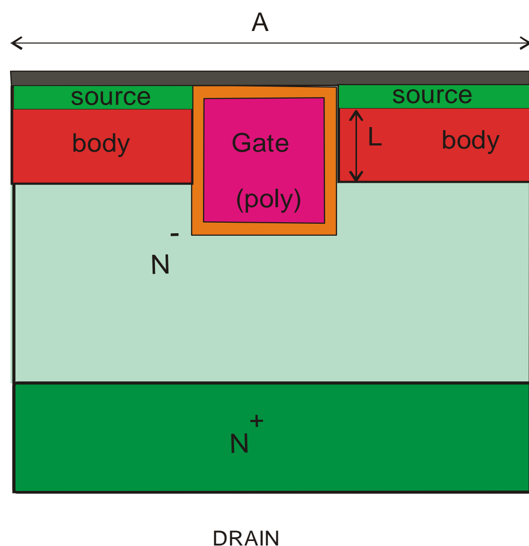


Fig. 10

To reduce furthermore the cell pitch A, without increasing the R_{JFET} component, it has been introduced the Trench MOS structure for the elementary cell, reported in figure.

Here the gate region is made by preferential etching of the the surface and making a trench. On the trench surface the gate oxide is grown, and then the trench is filled by polisilicon. In this way the cannel is made vertical across the body region, and there is no more JFET effect on the current.

By this structure the cell pitch A can be dramatically decreased respect to the planar case. As an example:

Planar VDMOS: A = 30 - 40 µm

Trench MOS: A = 6 µm

IV characteristics of the power MOS

The $I_D V_{DS}$ curves of a Power MOS are influenced by the R_{epi} that will add a voltage drop to the usual IV curves in the triode region, that can be quite relevant for high voltage MOS devices. A an example the output IV curves are reported in figure 11a, where the dashed curves refer to a low voltage MOS, while the solid line curves refer a high voltage MOS with an R_{ON} larger that the channel resistance.

The transfer curve (fig. 11b) presents a threshold voltage V_T of about 3 – 4 V. The larger V_T with respect to the signal MOS is due to the thicker gate oxide, needed to sustain the possible high voltage spikes induced on the gate during switching operation. t_{OX} of the order of 200 – 500 nm are used to avoid oxide breakdown and failure.

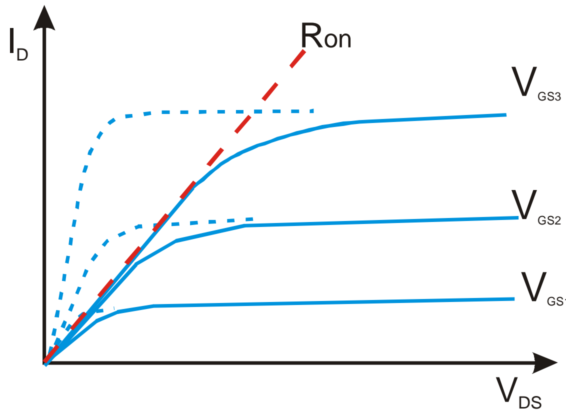


Fig. 11a – Output IV curves of a Power MOS

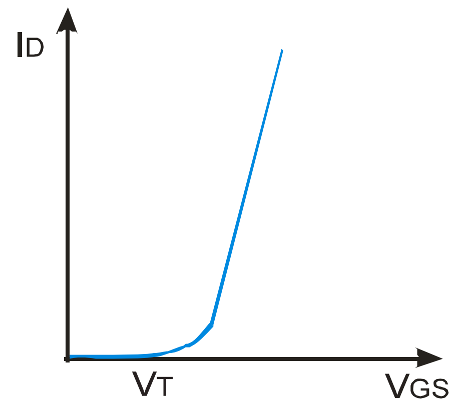


Fig. 11b Transfer curve

Temperature dependence of IV curves

The temperature effect on the IV curves can be understood with reference to the basic eq. (10a,b)

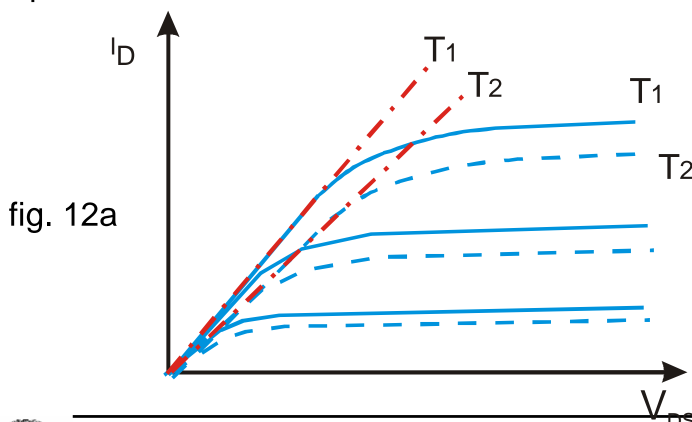
$$R_{ON} \cong R_{EPI} = \frac{W_D}{qA\mu_N(T)N_D} \quad (10a)$$

$$I_D = \frac{\mu_n(T)C_{OX}W}{2L}\left(V_{GS} - V_T(T)\right)^2 \quad (10b)$$

From (10a) we see that R_{ON} increases with temperature due to the reduction of mobility with temperature (fig. 12a).

From eq. (10b) the temperature increase has two contrasting effects on drain current I_D : the K scale factor decreases because the mobility is decreasing, but the threshold voltage V_T decreases, thus increasing the term under parenthesis. The latter effect is more important at low V_{GS} (low currents), as it can be seen in fig. (12b), while at high currents the former predominates.

fig. 12a



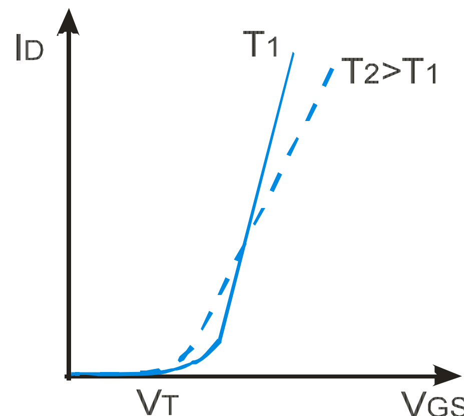


Fig. 12b

Recall the general condition for thermal instability seen before: $$\frac{dP_D}{dT} \geq \frac{dP_T}{dT}$$

where P_D = IV is the electrical power dissipation, and $P_T = dT/R_T$ is the thermal power dissipation dependent on the thermal resistance R_T; in the case of power MOS this conditions means:

$$V_{DS}\frac{dI_D}{dT} \geq \frac{1}{R_T(t)} \qquad \text{where} \qquad \frac{dI_D}{dT} \equiv \alpha(I) < 0 \qquad (11)$$

As seen in the previous thermal analysis, the current temperature coefficient $\alpha_T(I)$ for the power MOS is negative (at least for medium-high currents); then from eq. (11) we see that the MOS is intrinsically thermally stable: we can parallel safely the devices if a larger current is needed.

Also the large amount of elementary cells connected in parallel for a single discrete device is not detrimental in term of temperature uniformity of the chip.

Switching behavior of the VDMOS

In dynamic operation, we must consider that the power MOS is the merging of two integrated devices, as indicated in figure 13a:

a) the lateral MOS between the source N^+ layer and the epi layer
b) the vertical PIN diode between the body layer and the Drain N^+ substrate

The device dynamics must take into account the different capacities of the MOS structure, but for negative drain voltages also the PIN diode dynamics (and operation) must be taken into account. This latter can be considered as a flyback diode integrated into the VDMOS, as indicated in fig. 13b.

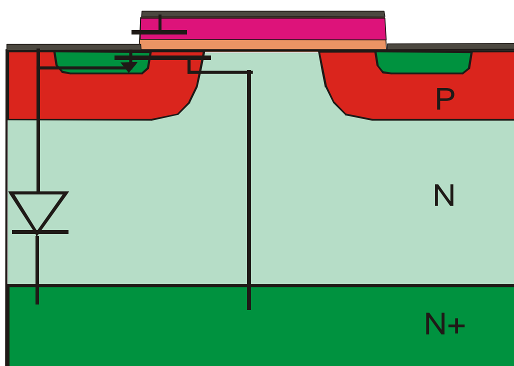


Fig. 13a

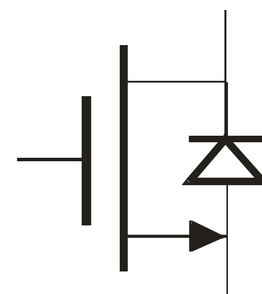
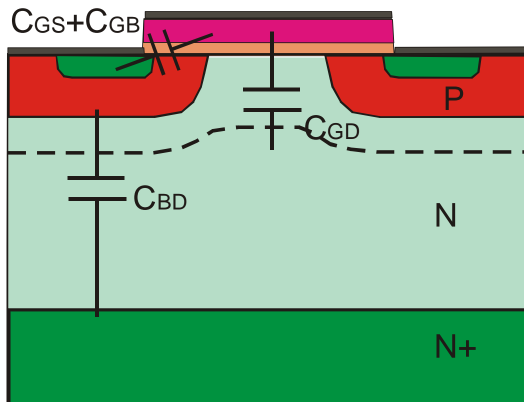
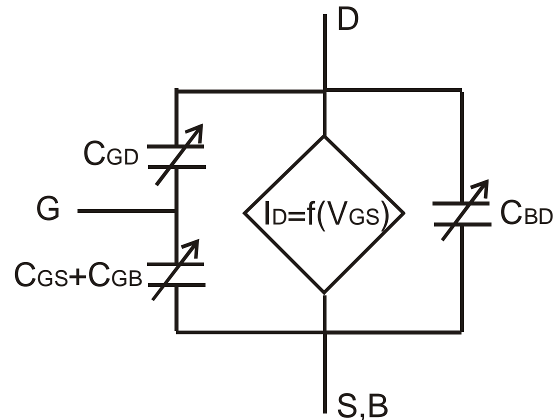


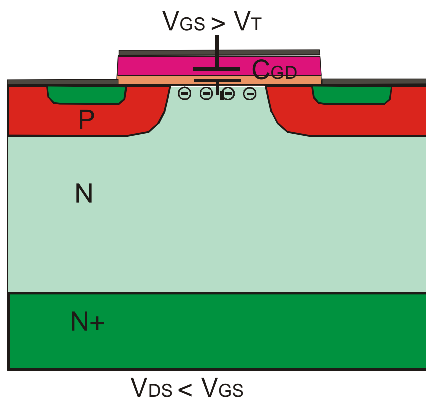
Fig. 13b

Capacitance components of the VDMOS

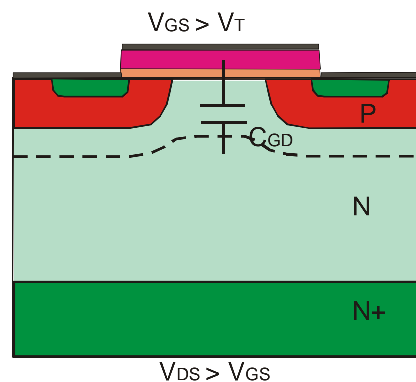
With respect to the gate capacitance components of the signal MOS, where the channel capacitances are the dominant ones, in the Power MOS there is an added components: C_{GD} generated by the gate area that lies above the intrinsic drain, i.e. the JFET region between the two body regions, that is much larger than the channel area.
This latter capacitance can be considered as the series of the oxide capacitance C_{ox} over the JFET region and the capacitance C_{DEPL} of the depletion layer created by the V_{DS} and V_{GS} voltages. This latter is strongly dependent on these voltages, that modify the carrier distribution in the N region between the two body regions and the depth of the depleted layer in that region, depending on the condition of the MOS operation.







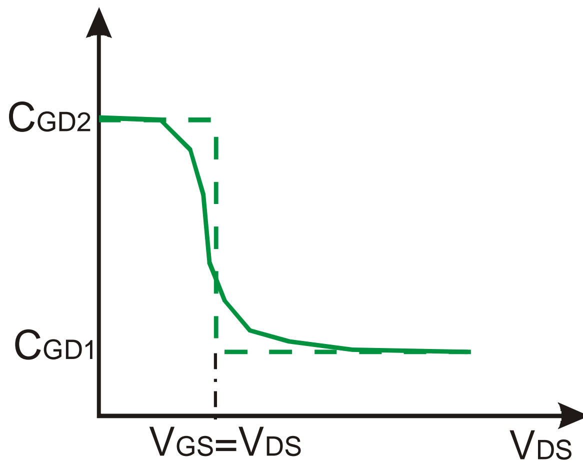
case a): $V_{DS} << V_{GS}$



case b): $V_{DS} >> V_{GS}$

There are two limiting cases for the capacitance C_{GD}:
Case a) for $V_{DS} << V_{GS}$; in this condition an accumulation layer of electrons forms underneath the oxide, so the depletion layer do not exist and the C_{GD} capacitance value coincides with C_{OX} and therefore it is very high
Case b) for $V_{DS} >> V_{GS}$,; in this case the carriers (electrons) are swept away from the surface and a depletion layer creates that increases with the drain voltage: as a result the C_{GD} value is mainly depending on the C_{DEPL} value, and it largely decreases due to the much higher thickness of the depletion layer compared to the thin oxide layer.

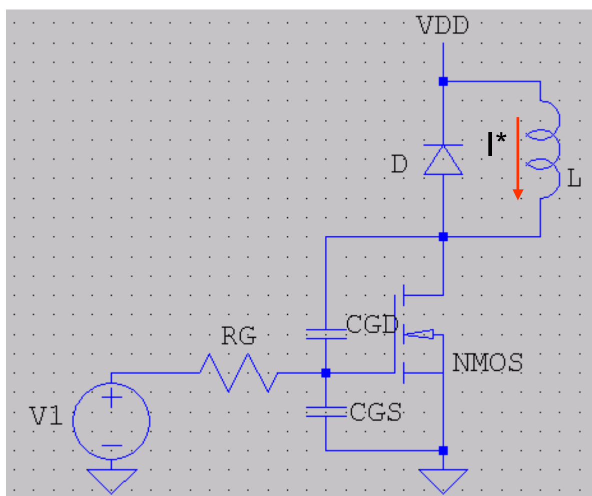
As a result, the capacitance C_{GD} varies of more of one order of magnitude when the drain voltage V_{DS} increase from values below V_{GS} to values above V_{GS}; the dependence of C_{GD} from V_{DS} is indicated in the plot of figure .
In the blocking state, where $V_{GS} < V_T$ and V_{DS} is large, the capacitance C_{GD} is at his minimum value C_{GD1}.



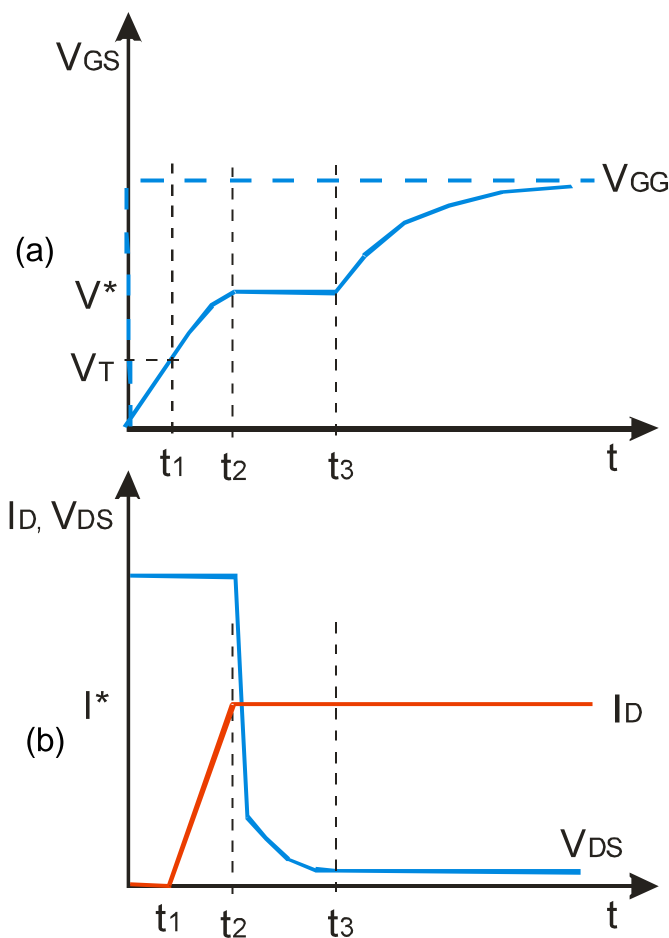
The variation of C_{GD} with gate and drain voltages has a significant effect on the switching behaviour of the power MOS, both in the turn-on and in turn-off switching waveforms, as we will see in the following.

Turn-ON on inductive load

For the turn-on of the power MOS with inductive load (and flyback diode, as assumed for all switching circuits), we assume a constant current I* flowing into the inductance L before the starting of the turn-on transient.
This current circulates into the diode D that is conducting, and the ON diode voltage V_D is about 1 V, i.e. negligible respect to the supply voltage V_{DD}. Then the initial value of the Drain Voltage is $V_{DS} \cong V_{DD}$. The gate voltage is kept to zero in the off state, so, before the turn-on, the capacitance C_{GD} is at the low value C_{GD1} ($V_{DS} >> V_{GS}$).



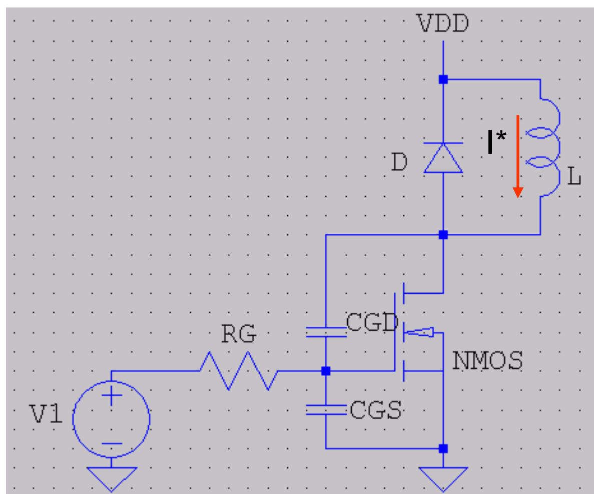
To start the turn-on transient, a positive voltage (usually 10 - 15 V) is applied to the gate by the drive circuit (here represented by an ideal voltage generator).
Due to the quite large input capacitance C_G , a series resistance R_G is needed in the input mesh to protect the drive circuit from an excessive current, due to the charge of the input capacitance C_G (usually some nF).
When the MOS start to conduct, a part of the current I* flows into the MOS and the current into the diode reduces down to zero when all the inductance current I* (still assumed constant during the switching transient) is flowing into the MOS.



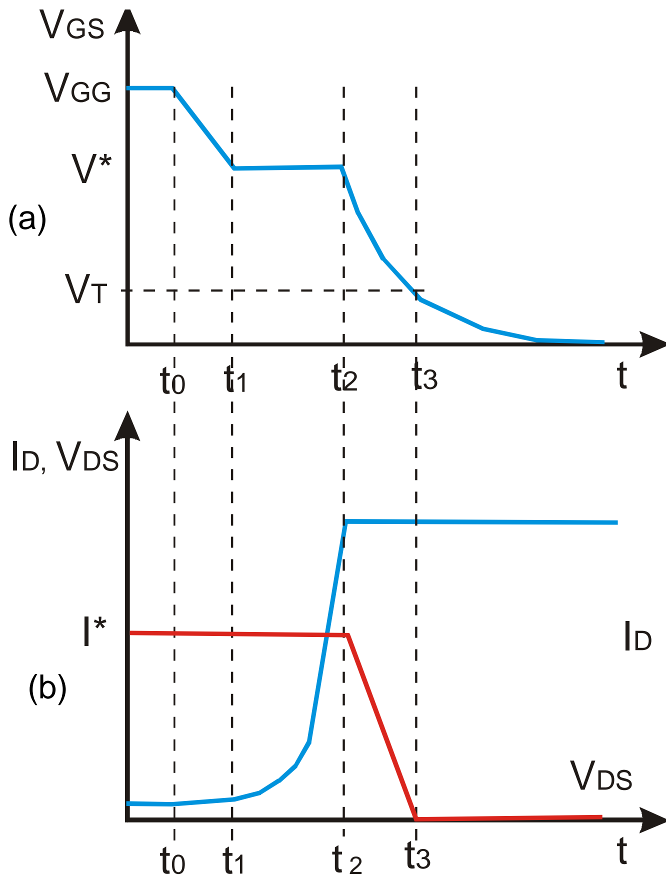
The schematic waveforms for V_{GS} (fig. a) and V_{DS}, I_D (fig. b) are reported here:
Starting the transient from time 0, V_{GS} increases depending on the time constant $R_G C_G$, initally with linear slope. At t_1 $V_{GS} = V_T$ and after t_1 the drain current start to increase (again linearly).
Between t_1 and t_2 I_D increases but is still lower than I*: then the diode D is still in on state (but his current is decreasing in time) and the drain voltage V_{DS} is still equal to V_{DD}.
At time t_2 the drain current reaches the limit value I*: after that time I_D remains constant at I* (all the inductance current flows in the MOS), and the diode D is in OFF state. Then V_{DS} start to decrease (the difference $V_{DD} - V_{DS}$ is the reverse voltage across the diode D).
Between t_2 and t_3 the voltage V_{GS} remains constant, because, from the transfer curve in pinch-off, if the drain current is constant also the gate voltage is constant. The drain voltage V_{DS} decreases quickly down the value $V_{DS} = V_{GS}$; after that point V_{DS} decreases much more slowly due to the large increase of C_{GD}. At time t_3 the MOS exit from pinch-off and enters in the linear region, so the gate voltage V_{GS} will increase up to the final value.

Turn-OFF on inductive load

The turn-off of the power MOS with inductive load will follow the same beahviour (reversing the starting and final conditions), as for the turn-on switching.
Again we assume a constant current I* flowing into the inductance L before the starting of the turn-off transient. The gate voltage is at its V_{GG} value and the drain voltage V_{DS} is the minimum one (less han V_{GG}) so, before the turn-off, the capacitance C_{GD} is at the high value C_{GD2} ($V_{DS} < V_{GS}$). The voltage drop across the inductance L : $V_{DD} - V_{DSMIN}$ keeps the diode D in OFF state, so all the inductance current flows into the MOS.



When the drive circuit brings V_1 at zero (or negative) value, the gate voltage V_{GS} start to decrease in a linear way, due to the discharge of C_G through R_G, but during this phase the MOS will conduct the same current I* forced by the inductance L, because the diode D will be still in OFF state until the drain voltage will reach the supply voltage V_{DD}.



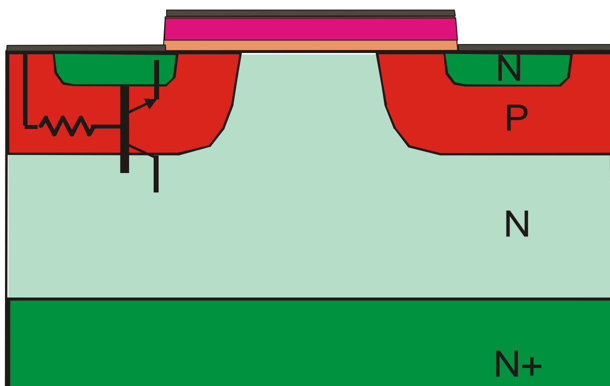
The schematic waveforms for V_{GS} (fig. a) and V_{DS}, I_D (fig. b) are reported here:

From t_0 to t_1 the output IV curves lie in the linear region , and the decrease of V_{GS} does not change too much the V_{DS} values. From t_1 the MOS enters in the pinch-off region; the drain current is still at I* and the V_{GS} is constant at the correponding value in the transfer curve. Due to the quite large input capacitance C_G V_{DS} will increase firstly in a slow way, but when V_{DS}>V_{GS} the capacitance C_{GD} decreases to C_{GD1}, and the drain voltage will increase at much faster rate.
At time t_2 V_{DS} reaches V_{DD} and the diode D will conduct; then the drain current I_D will decrease from I* to zero, when the gate voltage V_{GS} will reach the threshold value V_T

Max voltage ratings for Power MOS

The max voltages that the MOS can accept are:

a) at Gate terminal: the max voltage V_{GSMAX} is limited by the breakdown of the gate oxide. Typically it is in the range of 20 – 30 V, due to the t_{OX} thickness (about 20 -50 nm) larger than the one of signal MOS.
b) at Drain terminal: the max voltage V_{DSMAX} is limited by the breakdown of the body/drain junction. However the value of V_{DSMAX} can be reduced with respect to the breakdown value by some possible limiting effects due the parasitic BJT device already present in the power MOS structure.

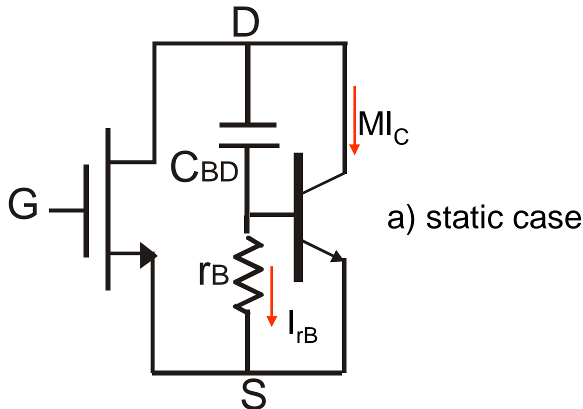


As indicated in the figure, the Nsource/Pbody/Ndrift regions actually constitute an NPN parasitic transistor. At a first analysis, this transistor has the base (Pbody region) short circuited to the emitter (source region) by the metal contact. However, due to the lateral width of the source region and to the resistivity of the body region, actually there is a distributed R_{body} resistance between the base and emitter, that could cause a turn-on of the BJT.

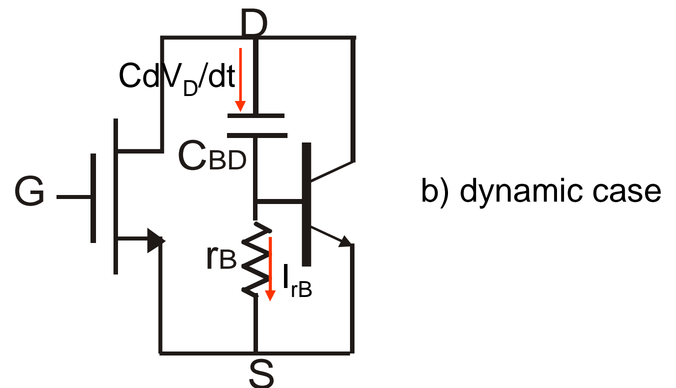
One must guarantee that the BJT will be always in off condition to avoid limitation in V_{DSMAX} due to the BV_{CE0} voltage instead to the BV_{CB0} voltage. The BJT can be brought in on state if a significant current I_{rB} could flow laterally into the body region toward the metallic body/source contact. This current will cause a voltage drop across the distributed resistance r_B, that can turn on the BJT if larger than 0.6 V.
With reference to the equivalent electrical circuit for the MOS + parasitic BJT depicted here, there are two possible causes for the current I_{rB}:

a) in static conditions, for V_{DS} near to the breakdown value, the BJT collector current due to avalanche multiplication flows into the body region and can give rise o a turn-on of the BJT.

b) in transient behaviour, the fast drain variation with time can induce a current in the capacity C_{BD} that will be again capable of turn-on the BJT.

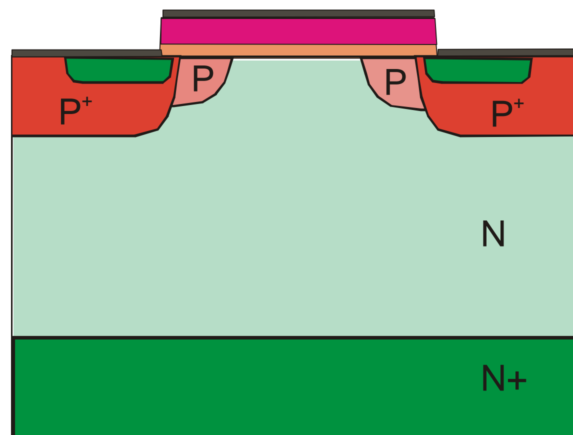


a) static case



b) dynamic case

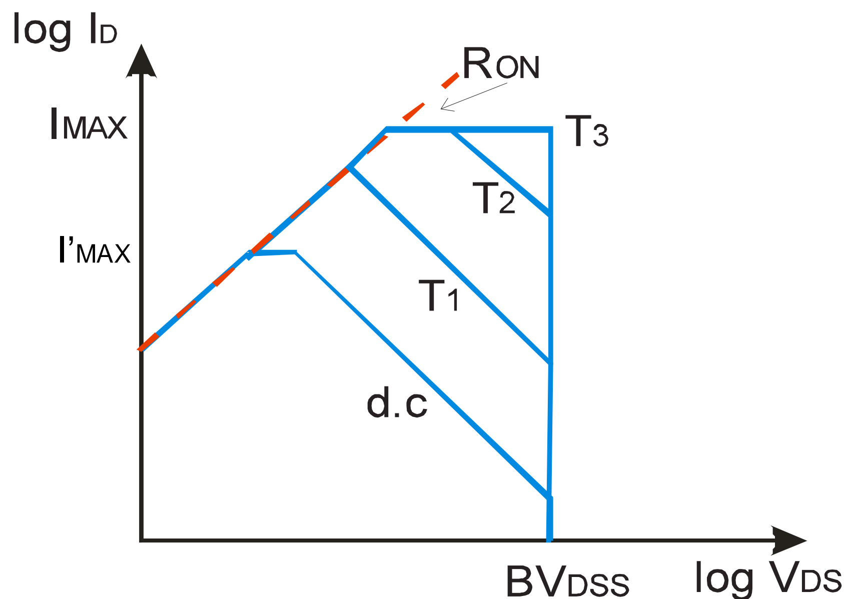
For both effects, to avoid the turn-on of the BJT one must reduce the voltage drop across the distributed resistance rB.
This can be accomplished by a double diffusion of the body region. The first one (P, indicated in figure with pink color) is done to define the channel and the doping of the channel region. The second one (P^+, indicated in figure with red color) is done in a reduced lateral region, underneath the source layer, with a larger doping and a larger depth, to reduce the spreading resistance r_B, and then reducing the possible turn-on of the parasitic BJT.



SOA of Power MOS

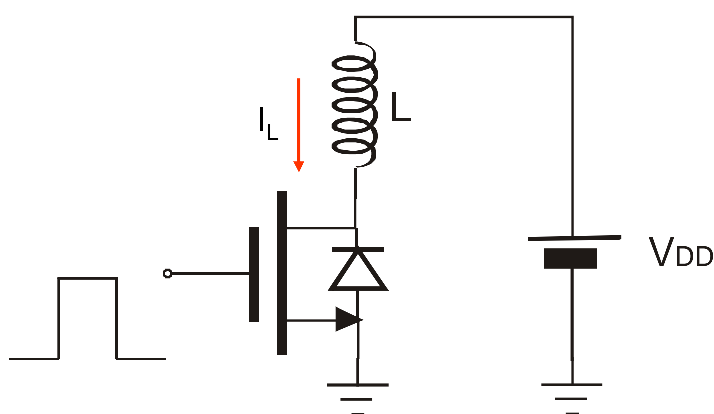
The S.O.A for Power MOS is limited by:

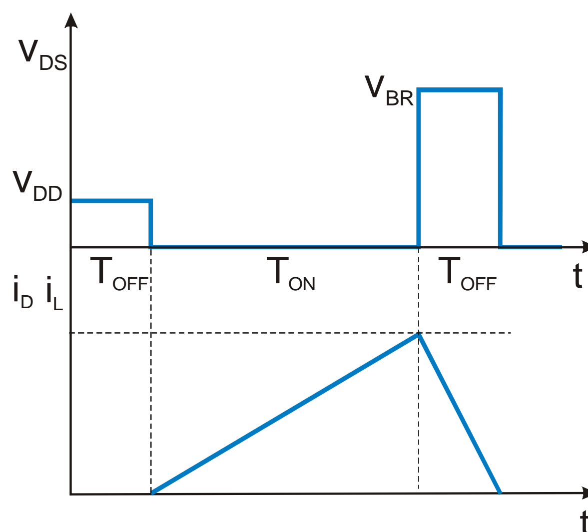
a) a max drain current I_{MAX} in d.c. case
b) a max current I'_{MAX} in pulsed condition
c) the ON resistance R_{ON} that limits the minimum Drain voltage
d) the max voltage V_{DSMAX} limited by the breakdown of the body/drain junction
e) a max constant power depending on the power pulse duration.



The Unclamped Inductive Switching (UIS) test

In some applications it is used an inductive load without any free wheeling diode, and during turn-off the MOS is brought into avalanche by the overvoltage generated across the inductance. In this mode of operation the intrinsic body diode of the Power MOS is used to absorb the energy stored in the inductance during avalanche conduction.
The test circuit used to evaluate the avalanche capability of the MOS during turn-off is named Unclamped Inductive Switching (UIS) test; it is used to evaluate the ruggedness of the device under this stress.





During T_{ON}: $$\frac{di_D}{dt} = \frac{V_{DD}}{L} \quad \Rightarrow \quad I_{DMAX} = \frac{V_{DD}}{L} T_{ON}$$

During T_{OFF}: $$\frac{di_D}{dt} = -\frac{V_{BR} - V_{DD}}{L}$$

Energy dissipated in the device:

$$E = \frac{1}{2} L I_{DMAX}^2 \frac{V_{BR}}{V_{BR} - V_{DD}}$$