COURSE DESCRIPTION
System on Chip

SSD: ELETTRONICA (ING-INF/01)

DEGREE PROGRAMME: INGEGNERIA ELETTRONICA (M61)
ACADEMIC YEAR 2022/2023

COURSE DESCRIPTION

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GENERAL INFORMATION ABOUT THE COURSE

INTEGRATED COURSE: NOT APPLICABLE
MODULE: NOT APPLICABLE
CHANNEL: FG A-Z
YEAR OF THE DEGREE PROGRAMME: II
PERIOD IN WHICH THE COURSE IS DELIVERED: SEMESTER I
CFU: 9

REQUIRED PRELIMINARY COURSES

none

PREREQUISITES

The course requires a basic knowledge of digital circuits, C programming language and one of the hardware description languages (VHDL or Verilog).

LEARNING GOALS

The objective of the course is the analysis and the design of complex electronics systems integrated within a single silicon chip. Such systems, while advantageous in terms of performance, require overcoming several issues related to the integration of heterogeneous circuits, the use of shared resources, the need to co-designing the hardware and the software parts of a complex application.
The course provides advanced methodologies for the design and the validation of a complex electronic system. Architectural optimization strategies are provided. Solutions for on-chip

communication are discussed and analyzed. Modern interfaces for off-chip communication are also thoroughly explained. The course also introduces to the state-of-the-art design technologies used in the industry.

EXPECTED LEARNING OUTCOMES (DUBLIN DESCRIPTORS)

Knowledge and understanding

By the end of the course the students must prove to own the following knowledge and understanding:

- advanced knowledge of a System on Chip architecture: memory mapped architectures, system bus, serial interfaces, memory organization, scheduler, accelerators architecture, error correction circuits

- advanced knowledge of the techniques used for the design and the validation of a System on Chip: SystemVerilog language, High-Level synthesis

- knowledge of the typical architectures for data-paths used in a System on Chip

- ability to evaluate the performance of a System on Chip and its sub-systems

Applying knowledge and understanding

The students must prove to be able to design simple systems based on the memory-mapped architecture.

The students must prove to be able to synthesize an accelerator using a software for the high-level synthesis.

The students must prove to be able to validate the functionality of a system using the SystemVerilog language.

The student must prove to be able to use industry standard tools for the development of System on Chip based on a programmable architecture, such as the Xilinx Zynq device.

COURSE CONTENT/SYLLABUS

Memory mapped architectures. Processing system of a programmable SoC. System bus architectures: AMBA bus, AXI protocol. High-level synthesis: allocation scheduling and binding, functional units and simple operators, static and dynamic floorplan, buffering, loop pipelining and unrolling, memory decomposition, dataflow architectures, handshaking, formal techniques. SystemVerilog: data types, clocking object, procedural statements, program object, concurrent programming, DPI, interfaces, assertions, classes, coverage. Serial interfaces: examples (IIC, SPI, JTAG, CAN), serial interfaces advantages and features, coding and scrambling, clock recovery, access methods, error detection and correction. Memory organization. Case studies: FFT accelerator, Computer Vision accelerator, audio elaboration, discrete cosine transform.

READINGS/BIBLIOGRAPHY

The course has no official textbook. The slides used during lessons, the laboratory guides and additional teaching material will be made available on the course webpage.

TEACHING METHODS OF THE COURSE (OR MODULE)

Oral lessons (50 hours) and lab sessions (30 hours). Lessons will be recorded and available for students.

EXAMINATION/EVALUATION CRITERIA

a) Exam type

- [ ] Written
- [x] Oral
- [ ] Project discussion
- [ ] Other

In case of a written exam, questions refer to

- [ ] Multiple choice answers
- [ ] Open answers
- [ ] Numerical exercises

b) Evaluation pattern